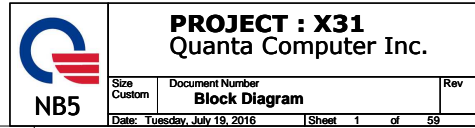
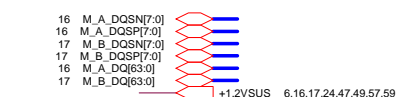


# 01

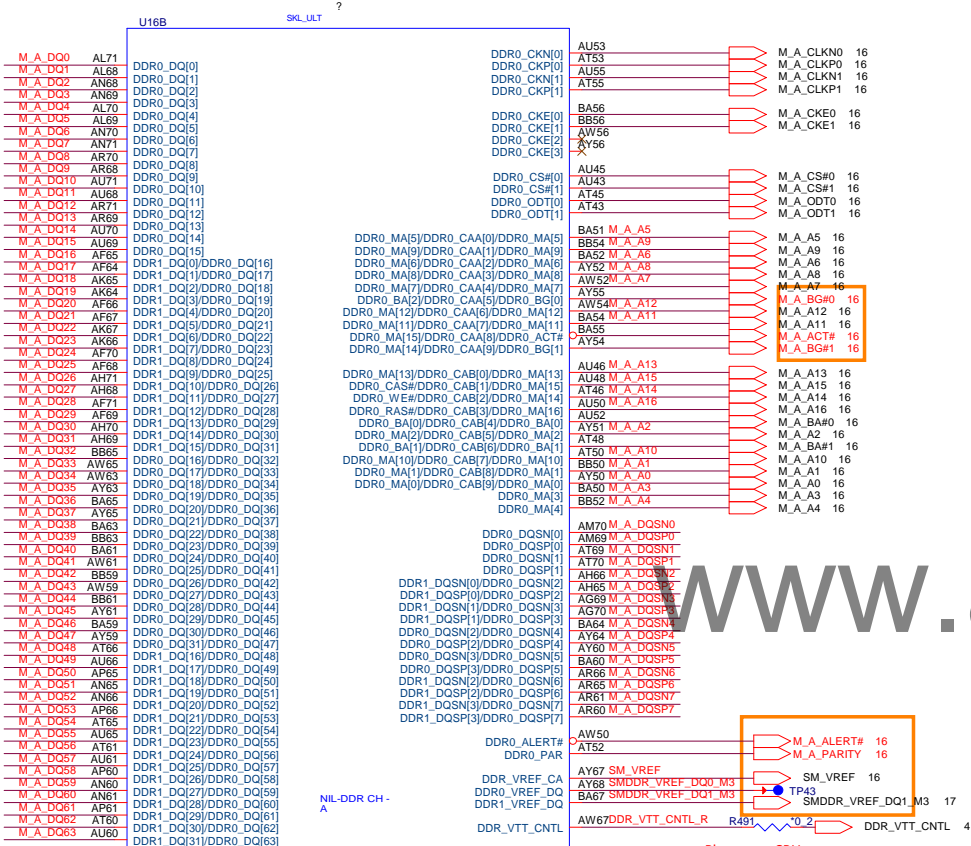




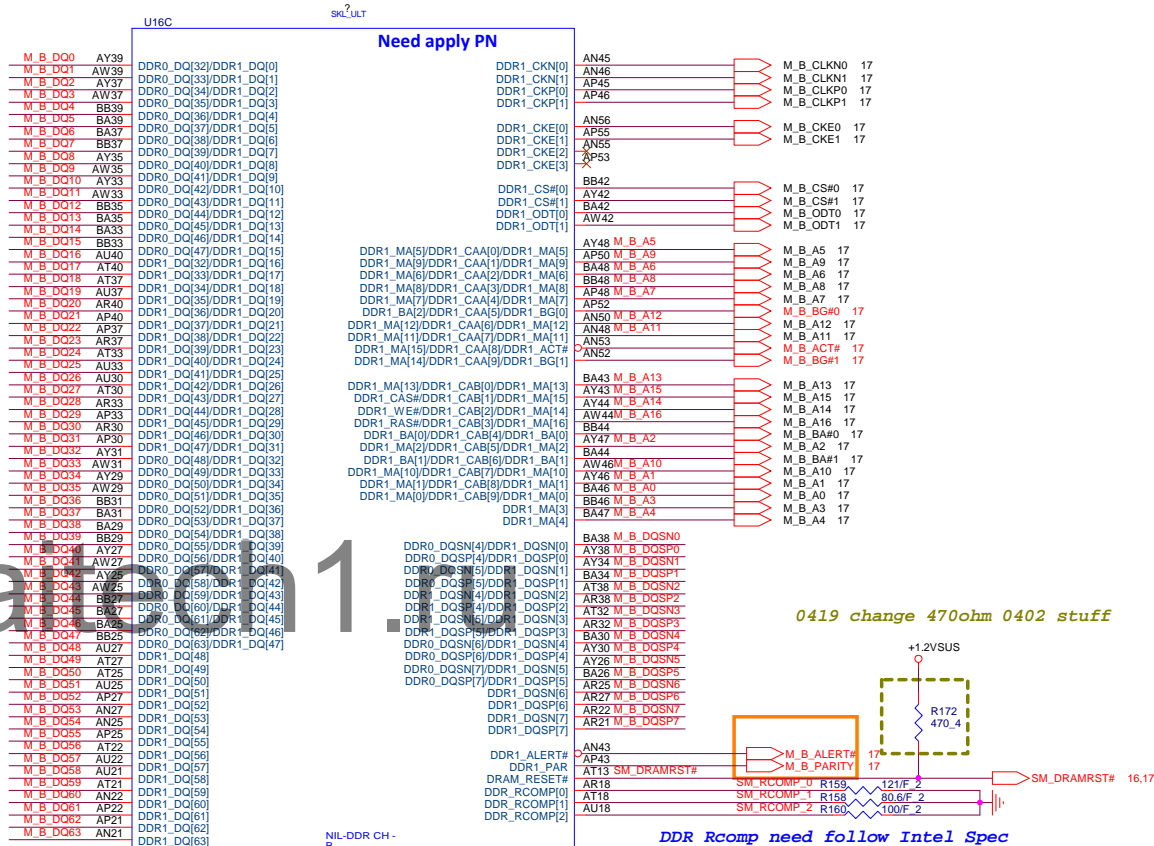
## KABYLAKE ULT Processor DDR4



Need apply PN



\*SKL\_ULT 2 OF 20  
REV = 1



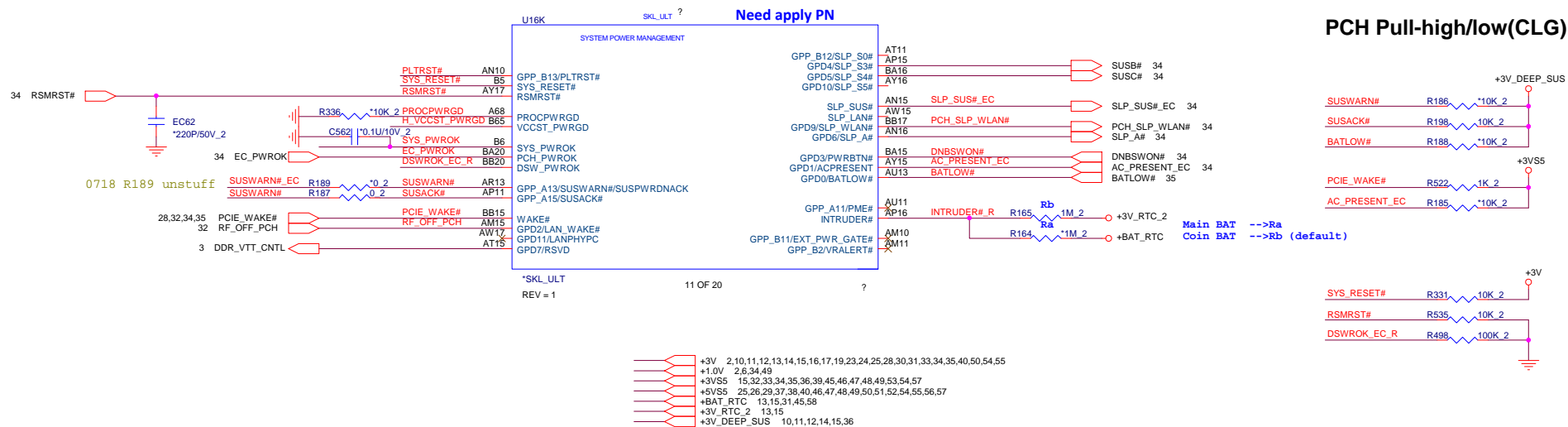
\*SKL\_\_ULT 3 OF 20  
REV = 1

**Table 4-34. KBL U DDR4/-RS SODIMM T3/8L Inline NIL Signal Routing Guidelines (Sh**  
2 of 3)

Signal Group	Region	Layer Route	Reference	Via Count	Trace Width (mils)	Target Impedance (Ω)		Min Trace Spacing (mils)				Max (mils) Length		R (0.05/16) (in)	
						Diff	Single Ended Tolerance (%)	Diff	Group	Group to Group (1&2)	Byte (1&2)	Region	Breakout		Total
RCOMP[0]	M	MS	VSS	2	12-15				20	25		500	500	121	
RCOMP[1]	M	MS	VSS	2	12-15				20	25		500	500	80.6	
RCOMP[2]	M	MS	VSS	2	12-15				20	25		500	500	100	

0419 change 470ohm 0402 stuff

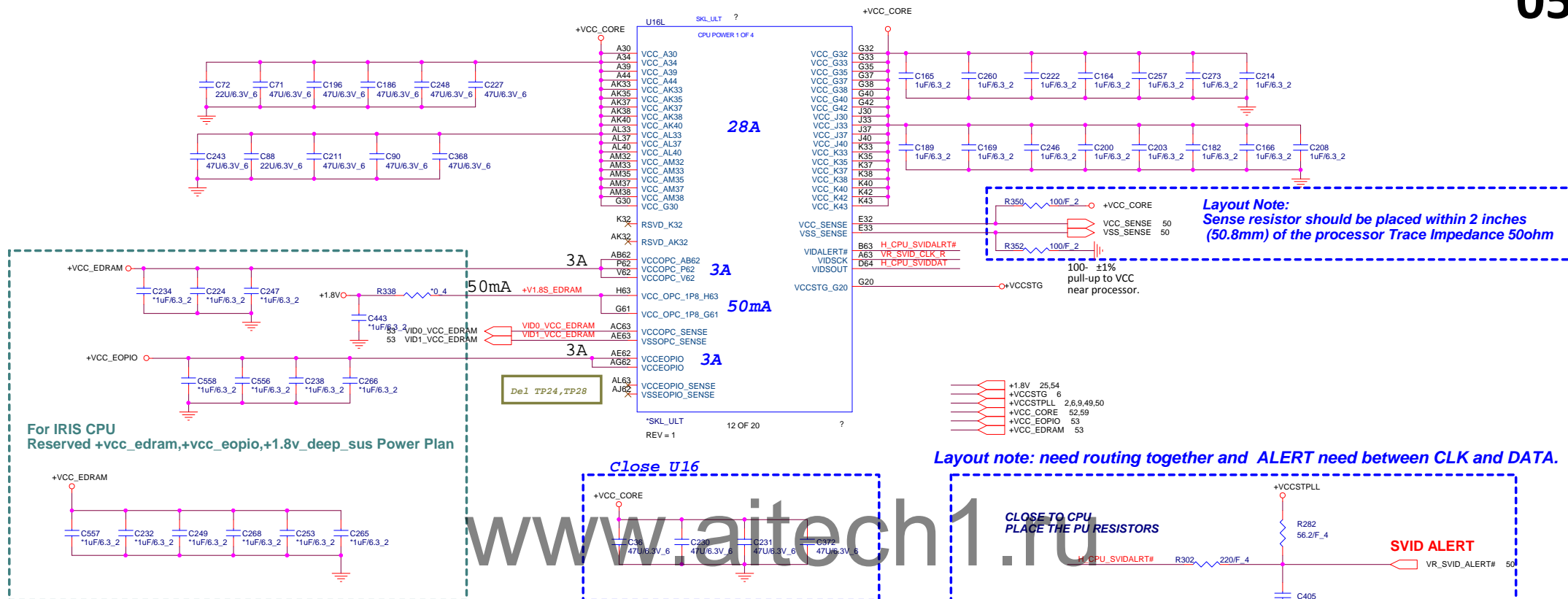
DDR Rcomp need follow Intel Spec  
12-15 min trance length

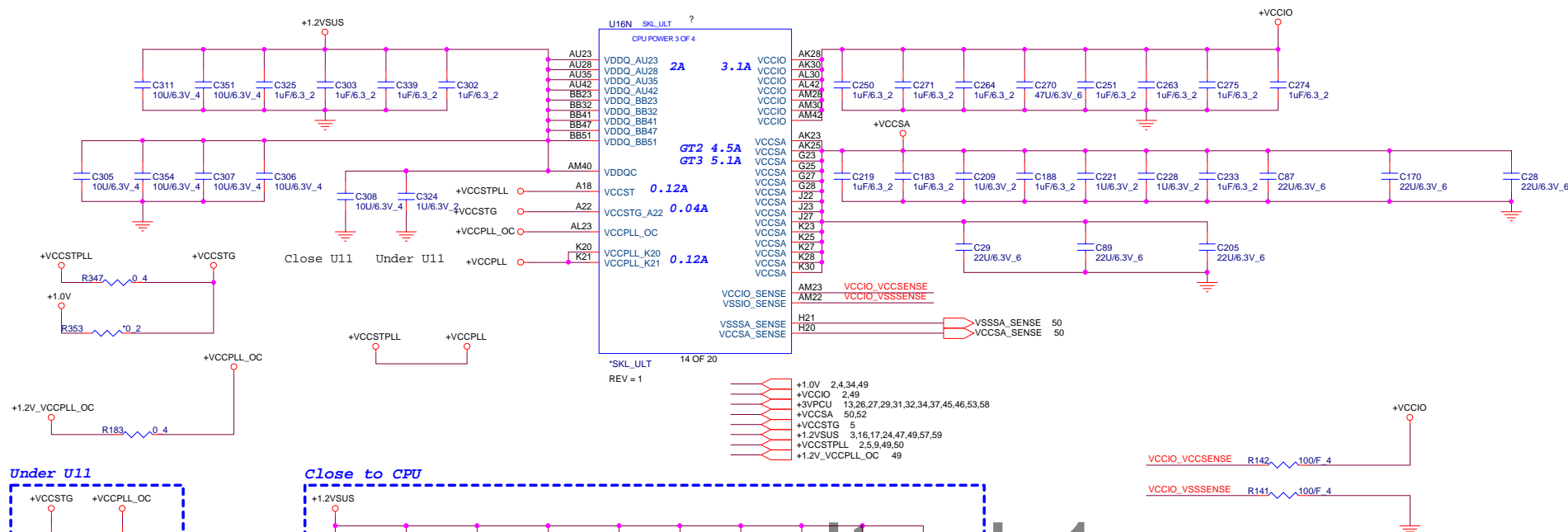


**PROJECT : X31**  
**Quanta Computer Inc.**

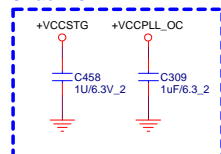
Size	Document Number	Rev
Custom	SKL U (3/14)	
Date: Tuesday, July 19, 2016	Sheet 4 of 59	



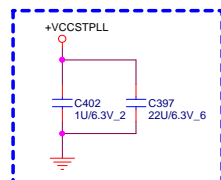




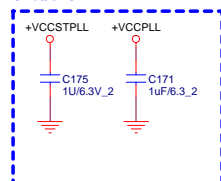
Under U11



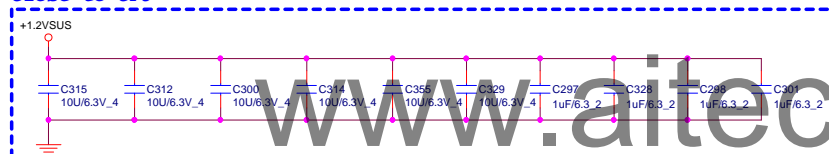
Close A18 Ball



Close U11

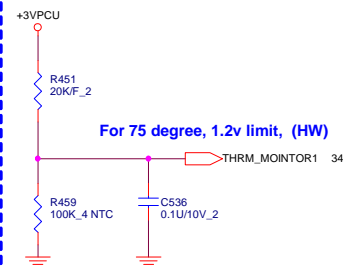


Close to CPU



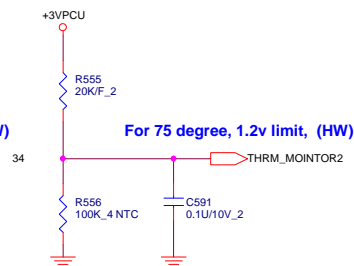
## CHOCK Ther Protect

For 65 degree, 1.8v limit, (SW)



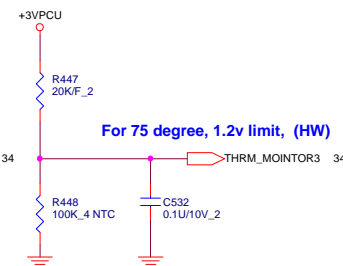
## DDR Ther Protect

For 75 degree, 1.2v limit, (HW)



## SSD Ther Protect

For 75 degree, 1.2v limit, (HW)

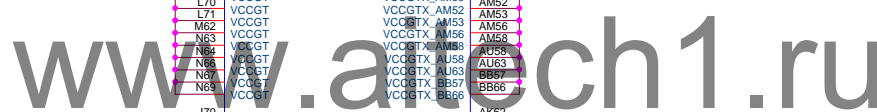


Power Rail	Description	Control
V <sub>CC</sub>	Processor IA Cores Power Rail	SVID
V <sub>CCGT</sub>	Processor Graphics Power Rails	SVID
V <sub>CCGTx</sub>	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V <sub>CCSA</sub>	System Agent Power Rail	SVID/Fixed (SKU dependent)
V <sub>CCIO</sub>	IO Power Rail	Fixed
V <sub>CCST</sub>	Sustain Power Rail	Fixed
V <sub>CCPLL</sub>	Processor PLLs power rail	Fixed
V <sub>DDQ</sub>	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V <sub>CCOPC</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCOPC_1P8</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCOPIO</sub>	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed




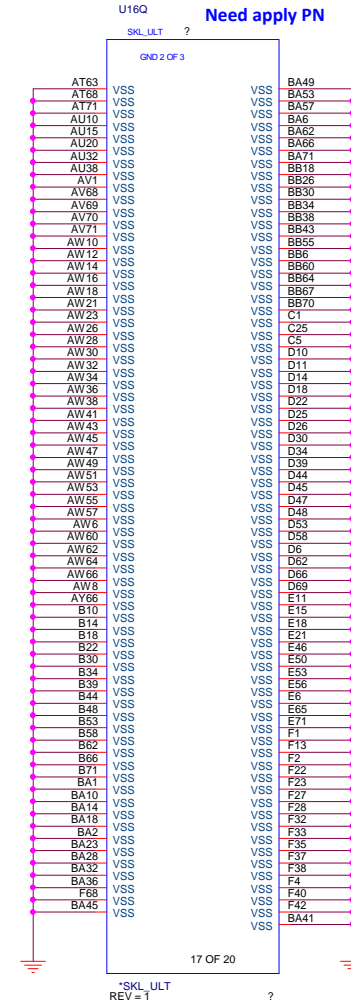
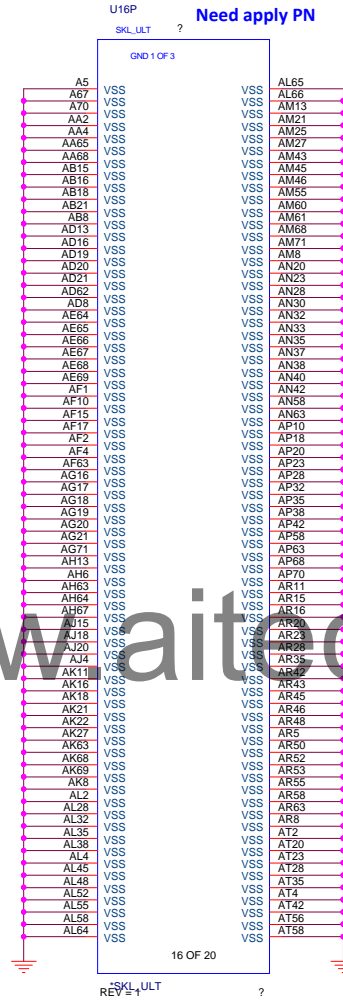
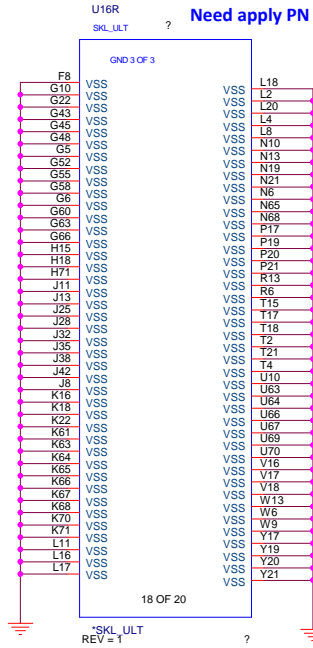
**PROJECT : X31**  
Quanta Computer Inc.

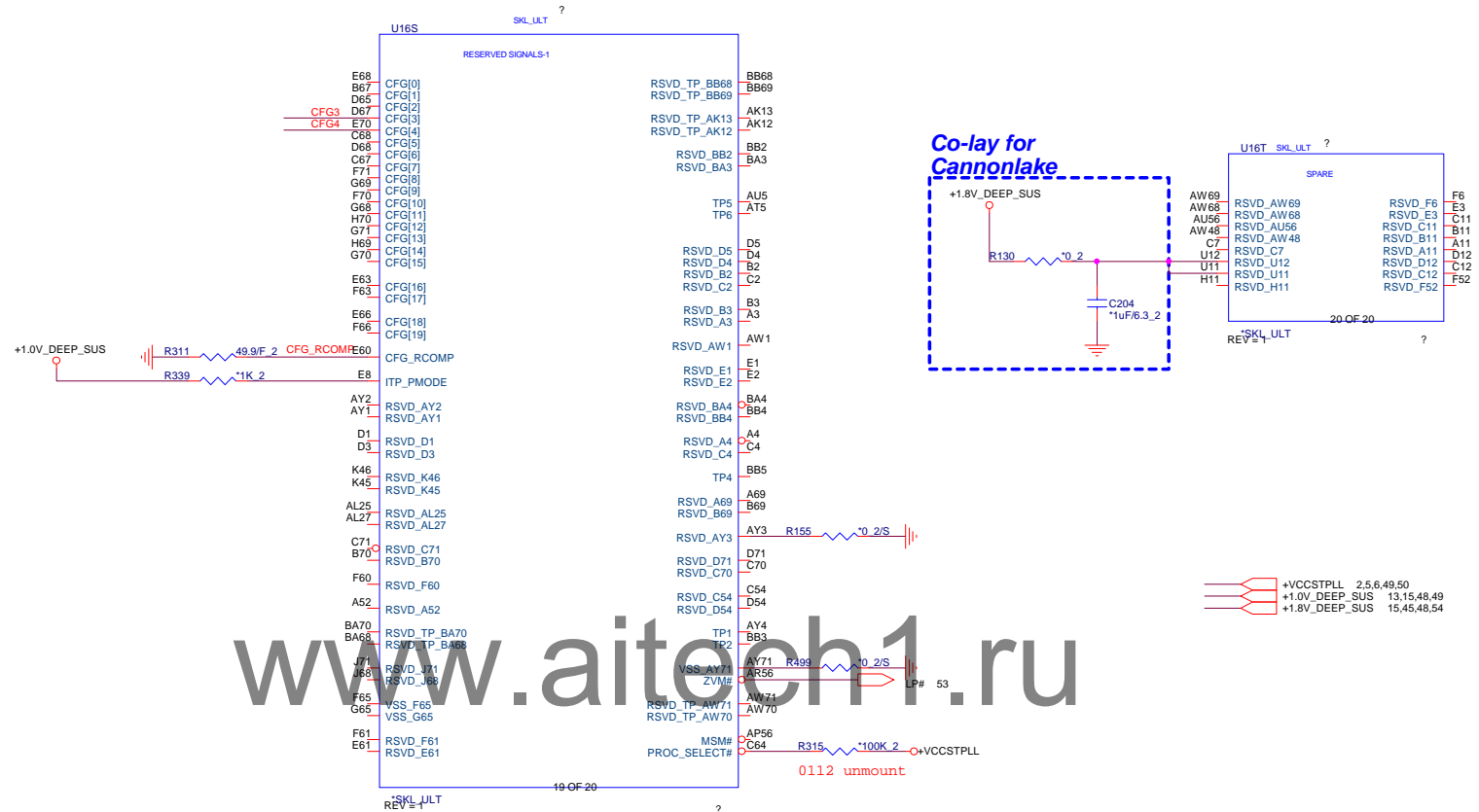
Size	Document Number	Rev
Custom	SKL U (5/14)	
Date: Tuesday, July 19, 2016	Sheet 6 of 59	



13 OF 20

	<b>PROJECT : X31</b> Quanta Computer Inc.		
	Size Custom	Document Number <b>SKL U (6/14)</b>	Rev
	Date: Tuesday, July 19, 2016		Sheet 7 of 59

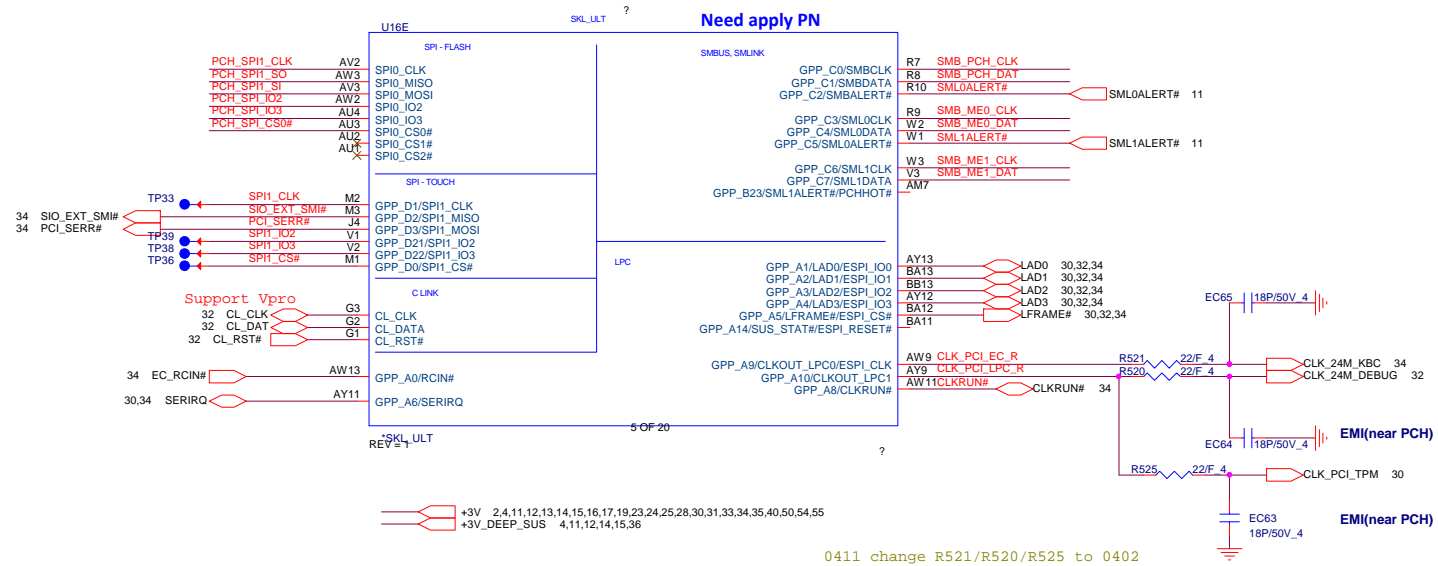




### Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (Physical Debug Enable) DFX_Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	CFG3 R346 1K 2
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	CFG4 R324 1K 2



## GPIO Pull UP

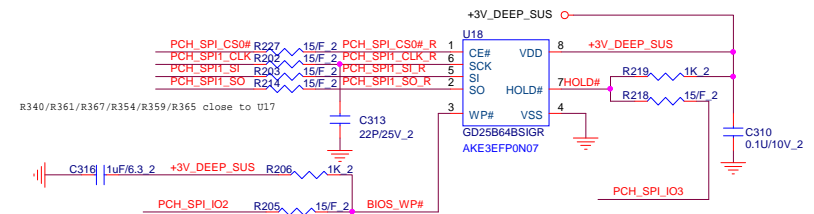
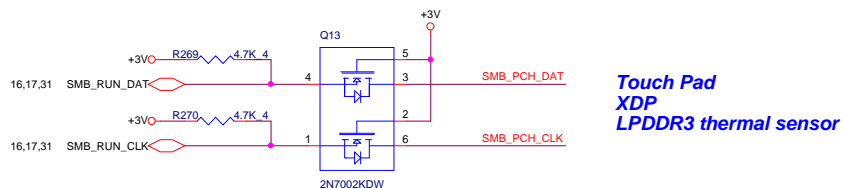


## PCH SPI ROM(CLG)

Vender	Size	P/N
EON	8MB	AKE3EZNOQ01 (EN25QH64-104HIP)
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE3EGN0Q01 (GD25B64BSIGR)
Socket		DFHS08FS023



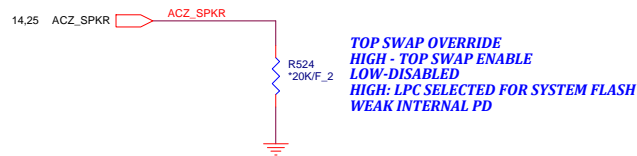
## SMBus/Pull-up(CLG)





# Functional Strap Definitions

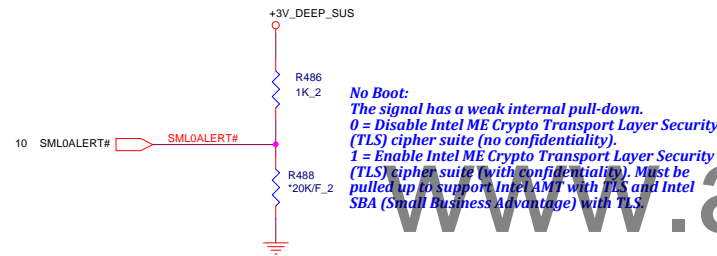
**DESIGN NOTE:**  
WEAK PULL UP RESISTOR PRESENT ON THIS NET



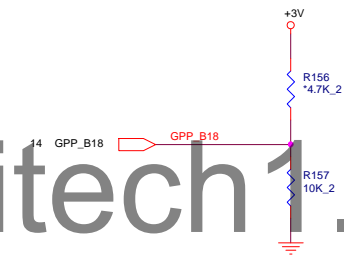
**TOP SWAP OVERRIDE**  
**HIGH - TOP SWAP ENABLE**  
**LOW-DISABLED**  
**HIGH: LPC SELECTED FOR SYSTEM FLASH**  
**WEAK INTERNAL PD**



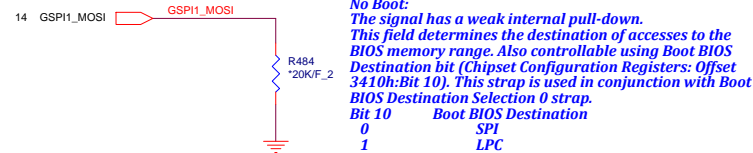
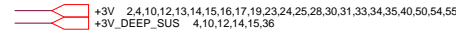
**No Boot:**  
The signal has a weak internal pull-down.  
0 = Enable security measures defined in the Flash Descriptor.  
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. This function is useful when running ITP/XDP.



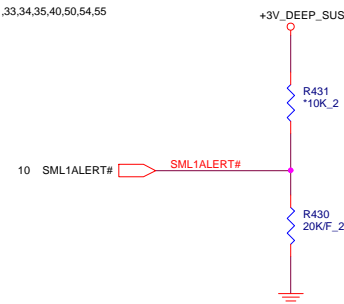
**No Boot:**  
The signal has a weak internal pull-down.  
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).  
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.



**No Boot:**  
The signal has a weak internal pull-down.  
0 = Disable No Reboot mode.  
1 = Enable No Reboot mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.



**No Boot:**  
The signal has a weak internal pull-down.  
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.  
**Bit 10**      **Boot BIOS Destination**  
0              SPI  
1              LPC

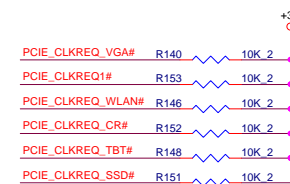
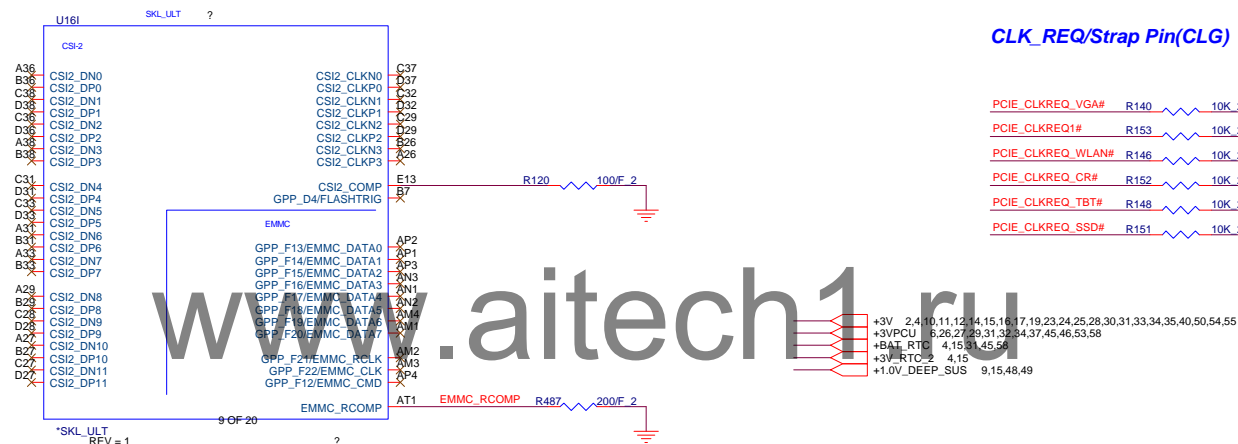
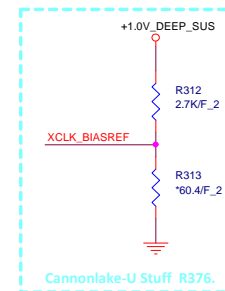


**No Boot:**  
The signal has a weak internal pull-down.  
0 = LPC Is selected for EC.  
1 = eSPI Is selected for EC.

\*SKL\_ULT  
REV = 1

+3V 2,4,10,11,13,14,15,16,17,19,23,24,25,28,30,31,33,34,35,40,50,54,55  
+3V DEEP SUS 4 10 11 14 15 36

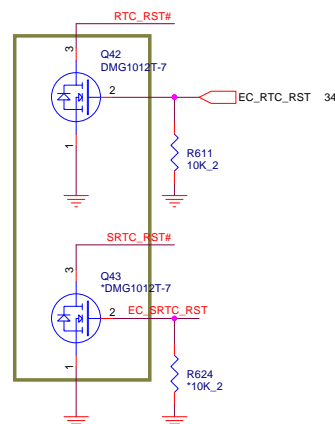
Un-used OC# need add pull high



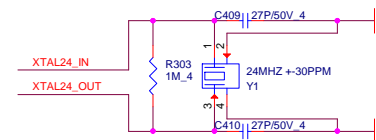
1



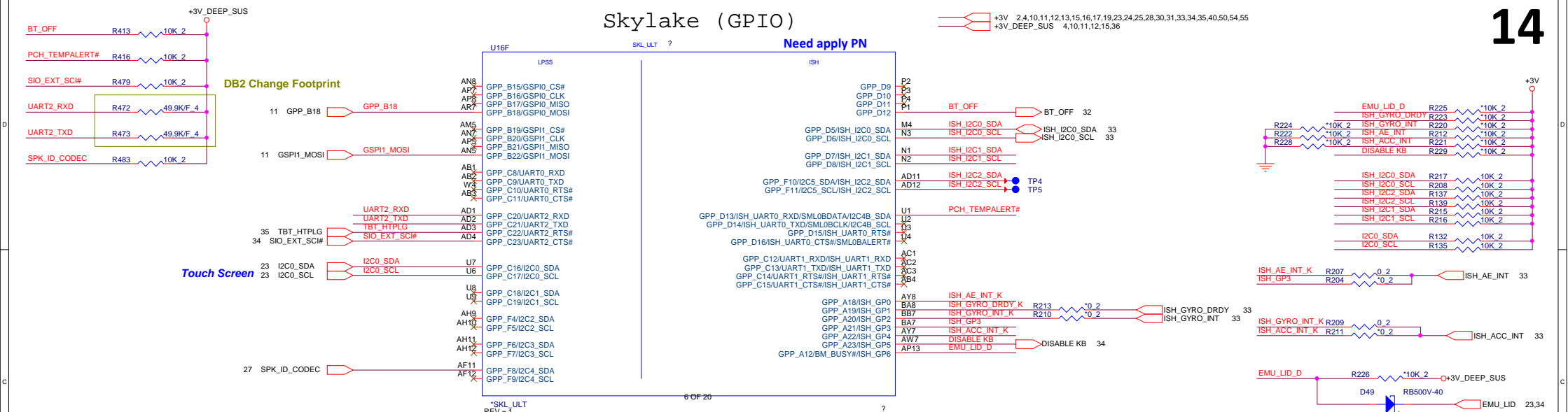
## 4



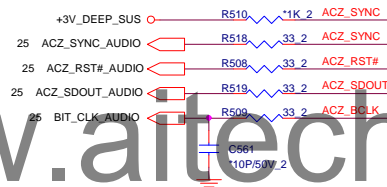
---



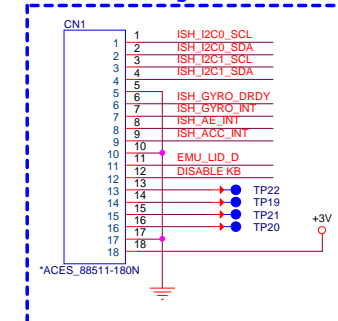
## Skylake (GPIO)



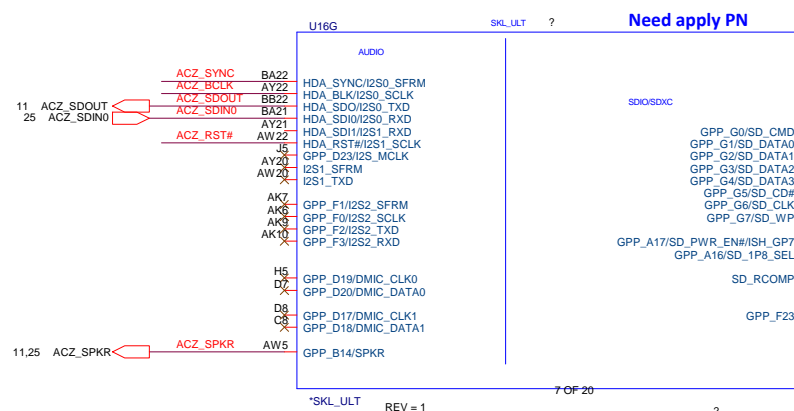
## HDA Bus(CLG)

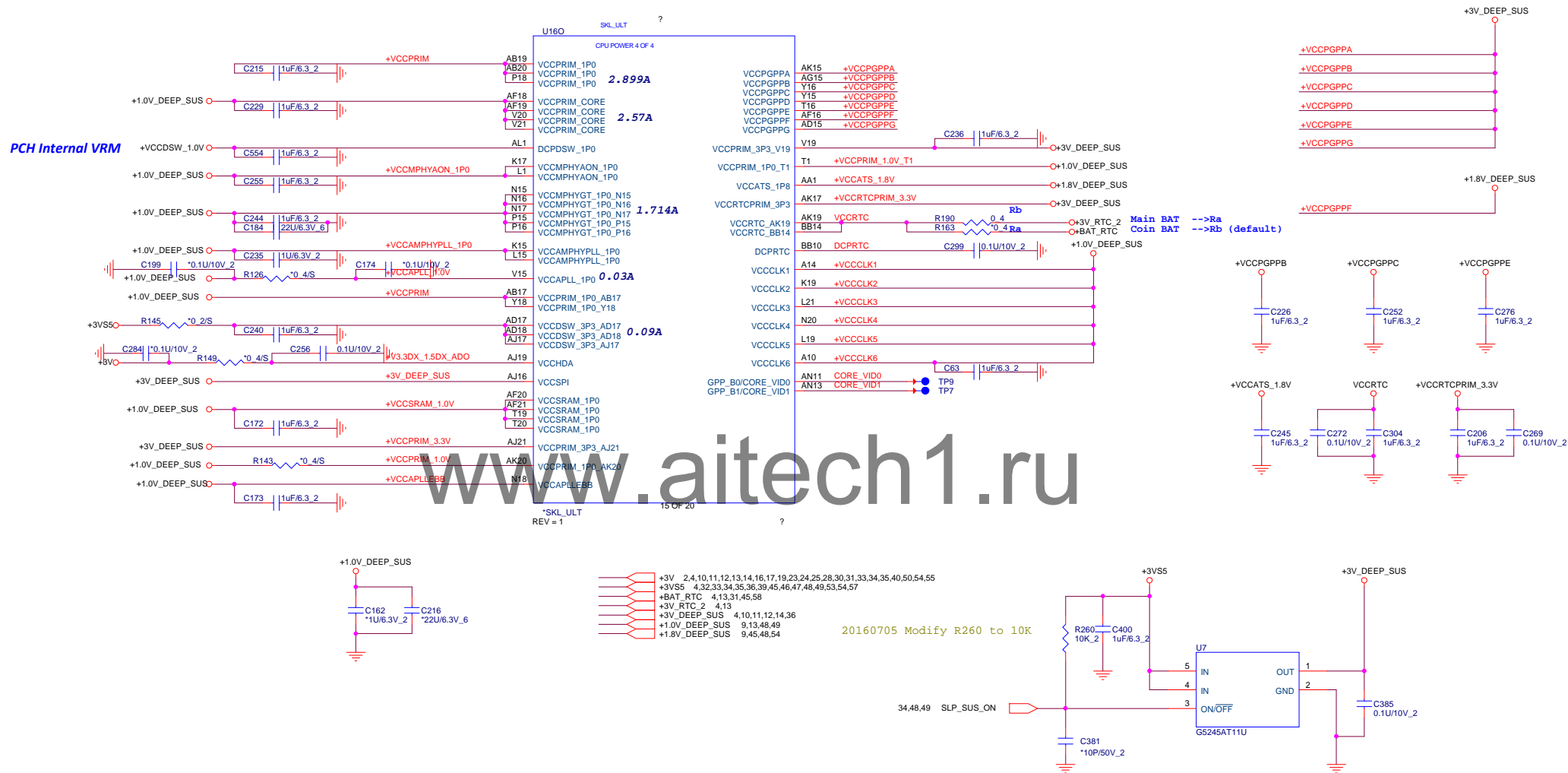


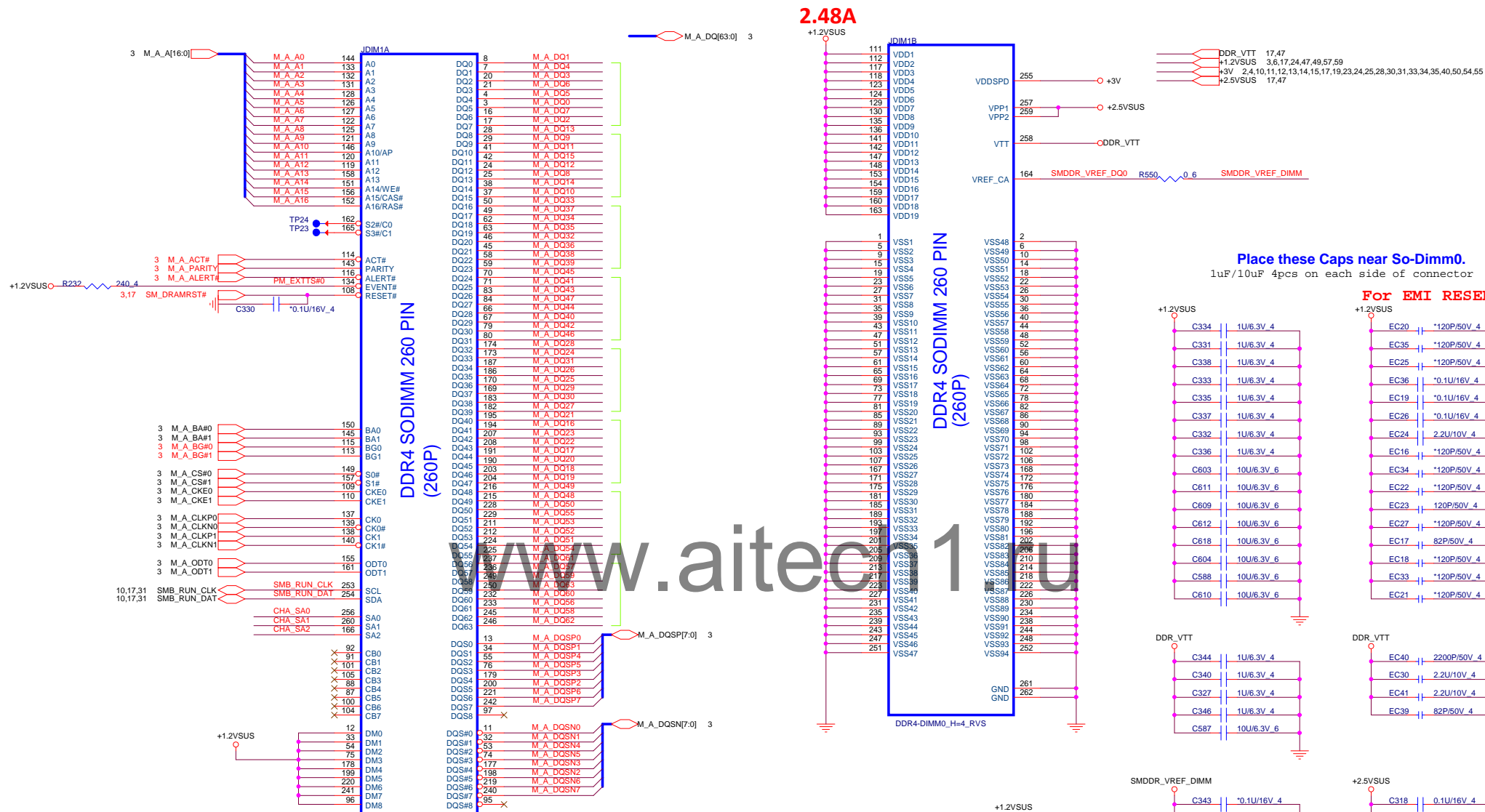
## Sensors Debug CONN



KBL-U	BOARD_ID8	BOARD_ID7	BOARD_ID6	Board ID [5:4]	BOARD_ID[3:0]				
Model	ID8	ID7	ID6	ID5 ID4	ID3	ID2	ID1	ID0	
X32	0 VPRO 1 Non VPRO	0 2+2 CPU 1 2+3E CPU	0 ESH 1 ISH	0 DIS (Default = 01)	0	0	0	0	Hynix 8Gb
					0	0	0	1	Samsung 8Gb
					0	0	1	0	Micron 8Gb
					0	0	1	1	Hynix 16G
					0	1	0	0	Samsung 16G
					0	1	0	1	Micron 16G
					0	1	1	1	
					1	0	0	0	
					1	0	0	1	
					1	0	1	0	
					1	0	1	1	

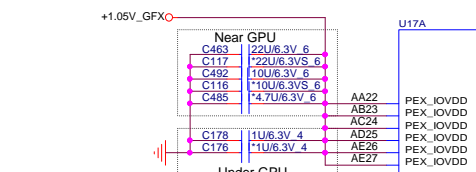




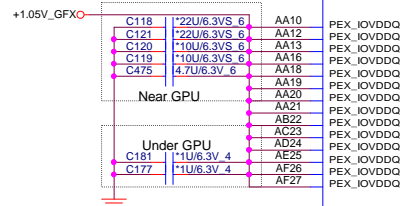




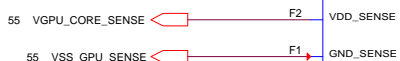
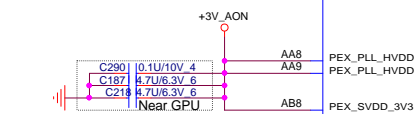




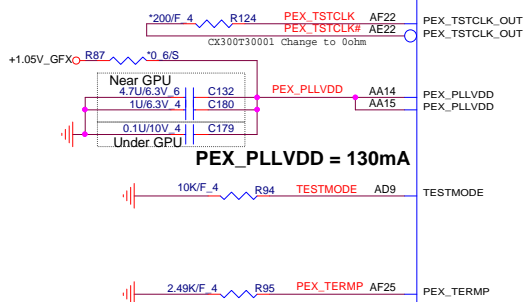
PEX\_IOVDD + PEX\_IOVDDQ = 1.042A



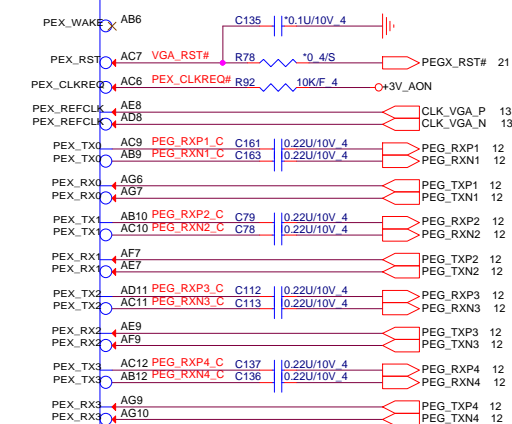
PEX\_PLL\_HVDD +  
PEX\_SVDD\_3V3 = 143mA



0611  
Change R433 to short pad



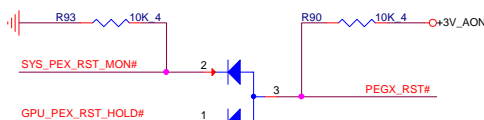
PEX\_PLLVDD = 130mA



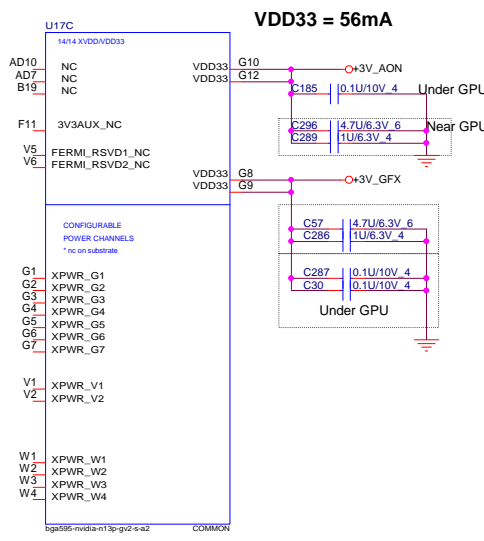
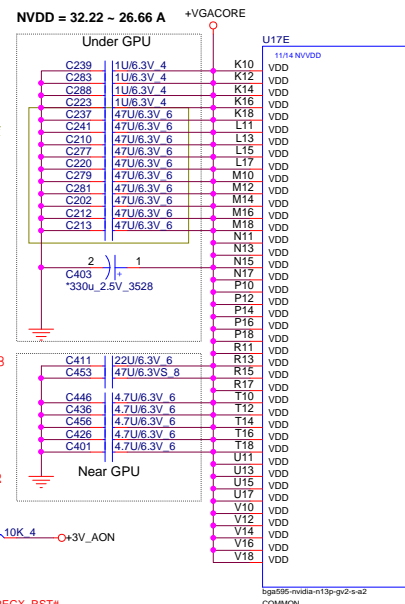
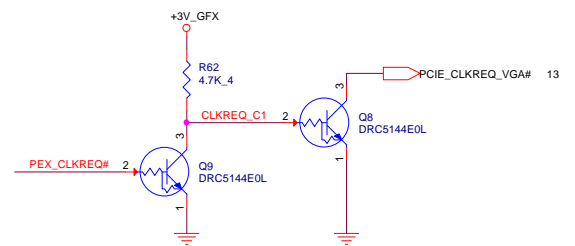
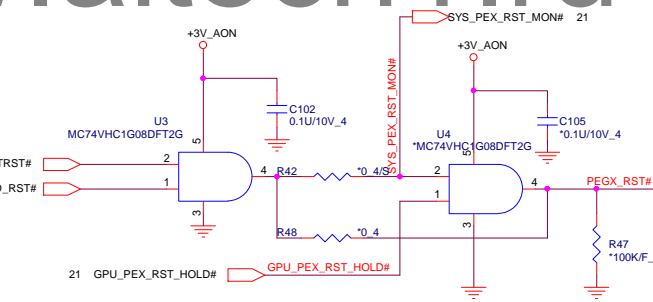
0602 Change  
4.7uF to 47uF

1230 Change C338  
size to 0603

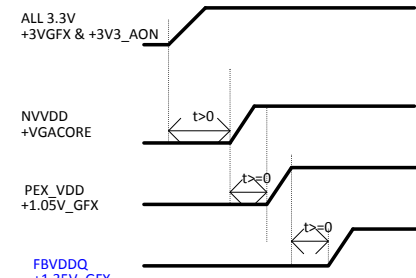
1230 Change C395,  
C370, C386, C349,  
C403 size to 0402



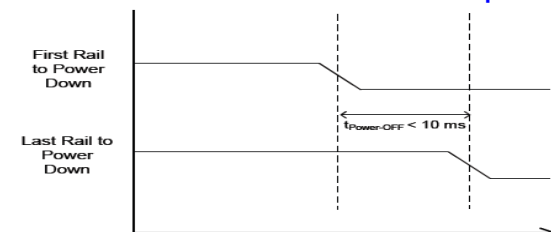
0611  
Change R196, R155 to short pad

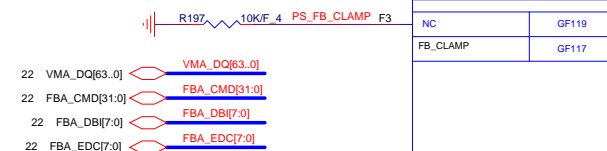


Power up sequence



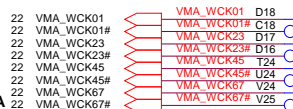
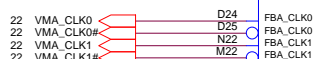
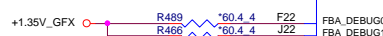
Power down sequence



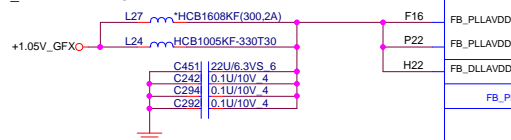


0310 Del  
R631/R644/R612/R670/R600  
for nVIDIA review

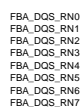
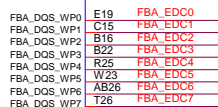
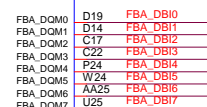
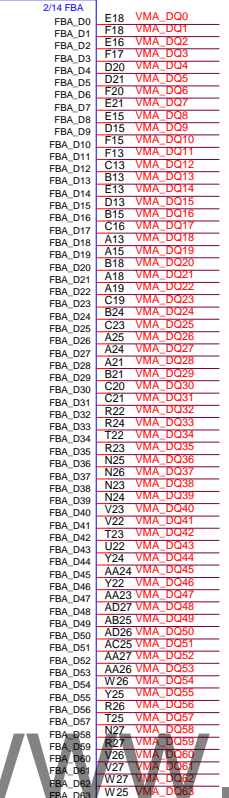
FBA\_CMD0 C27 FBA\_CMD0  
FBA\_CMD1 C26 FBA\_CMD1  
FBA\_CMD2 E24 FBA\_CMD2  
FBA\_CMD3 F24 FBA\_CMD3  
FBA\_CMD4 D27 FBA\_CMD4  
FBA\_CMD5 D26 FBA\_CMD5  
FBA\_CMD6 F25 FBA\_CMD6  
FBA\_CMD7 F26 FBA\_CMD7  
FBA\_CMD8 F23 FBA\_CMD8  
FBA\_CMD9 G22 FBA\_CMD9  
FBA\_CMD10 G23 FBA\_CMD10  
FBA\_CMD11 G24 FBA\_CMD11  
FBA\_CMD12 F27 FBA\_CMD12  
FBA\_CMD13 G26 FBA\_CMD13  
FBA\_CMD14 G27 FBA\_CMD14  
FBA\_CMD15 G26 FBA\_CMD15  
FBA\_CMD16 M24 FBA\_CMD16  
FBA\_CMD17 M23 FBA\_CMD17  
FBA\_CMD18 K24 FBA\_CMD18  
FBA\_CMD19 K23 FBA\_CMD19  
FBA\_CMD20 M27 FBA\_CMD20  
FBA\_CMD21 M26 FBA\_CMD21  
FBA\_CMD22 M25 FBA\_CMD22  
FBA\_CMD23 K26 FBA\_CMD23  
FBA\_CMD24 K22 FBA\_CMD24  
FBA\_CMD25 J23 FBA\_CMD25  
FBA\_CMD26 J25 FBA\_CMD26  
FBA\_CMD27 J24 FBA\_CMD27  
FBA\_CMD28 K27 FBA\_CMD28  
FBA\_CMD29 K25 FBA\_CMD29  
FBA\_CMD30 J27 FBA\_CMD30  
FBA\_CMD31 J26 FBA\_CMD31



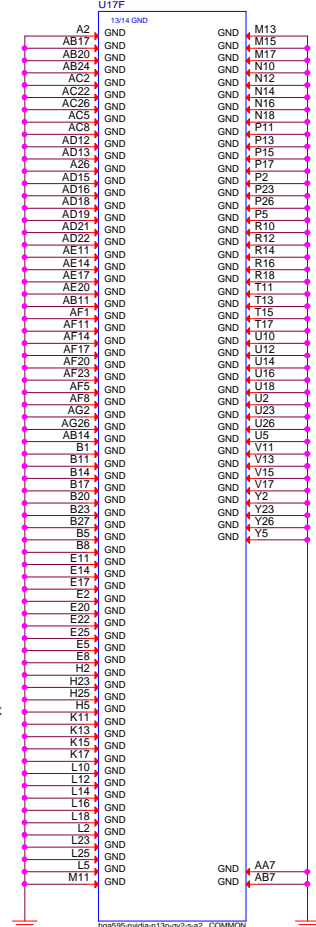
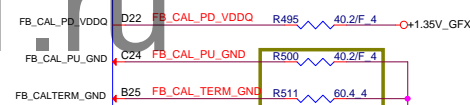
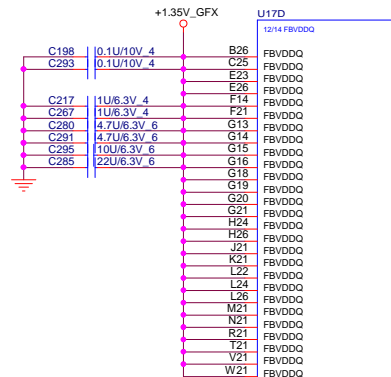
FB\_PLLAVDD = 55mA  
FB\_DLLAVDD = 15mA



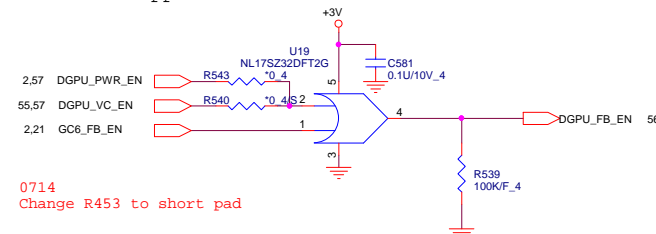
lga595-nvidia-n13p-gv0-s-a2

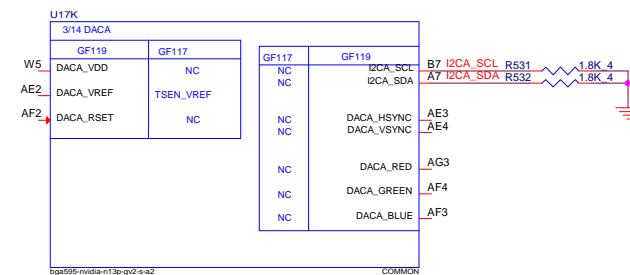
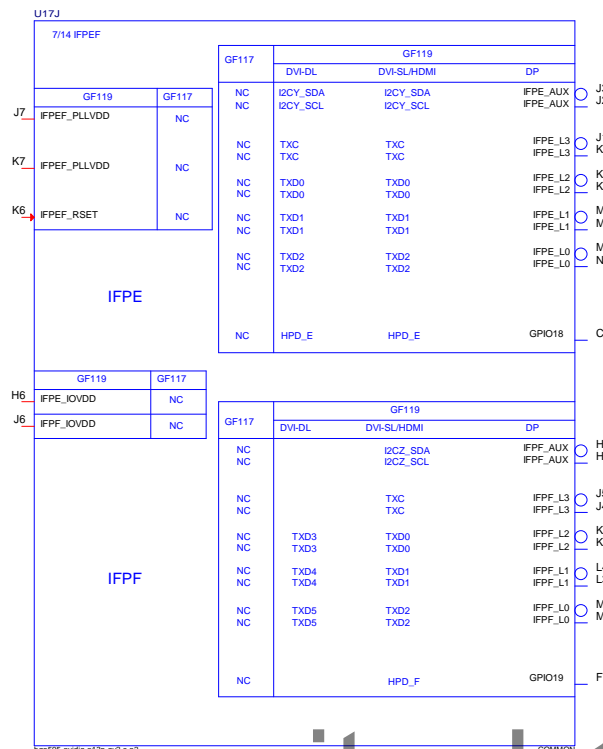
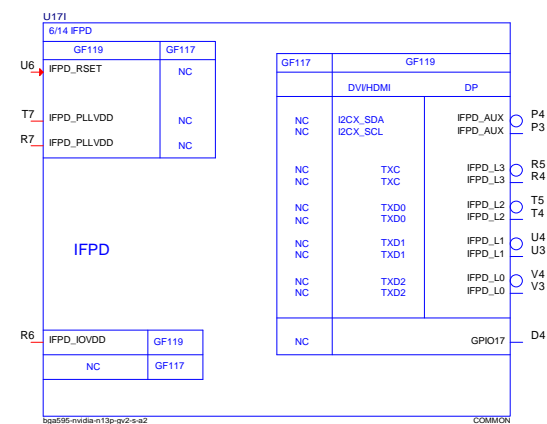
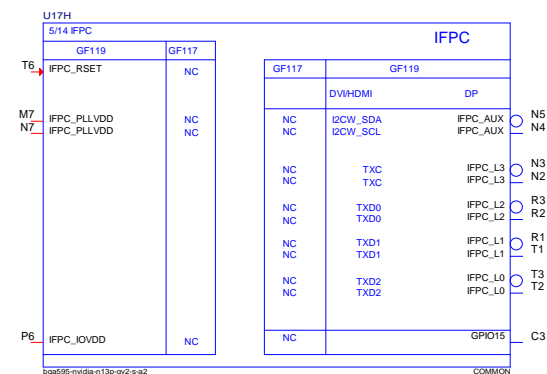
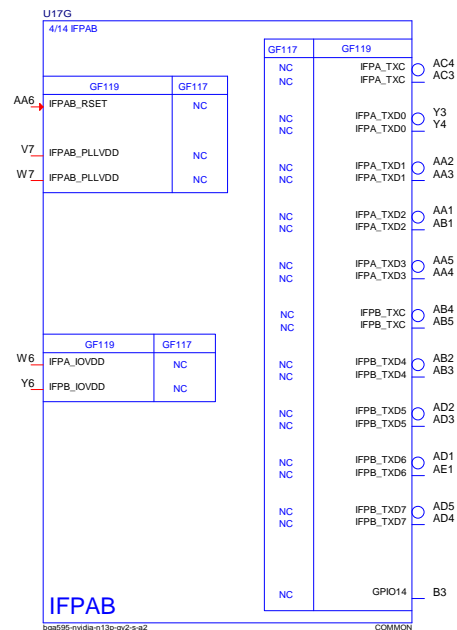


FBVDDQ + FBVDD = 3.116A

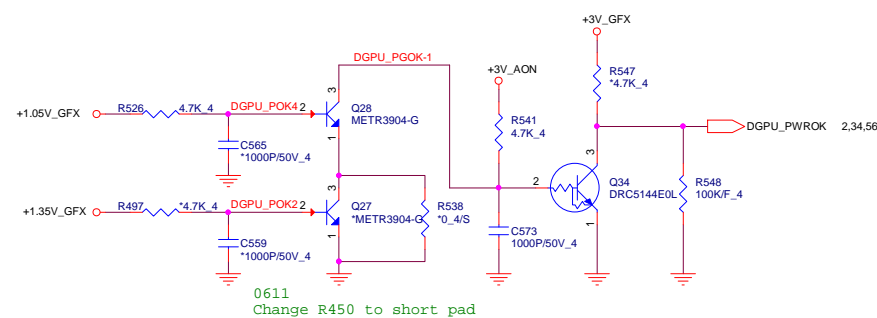
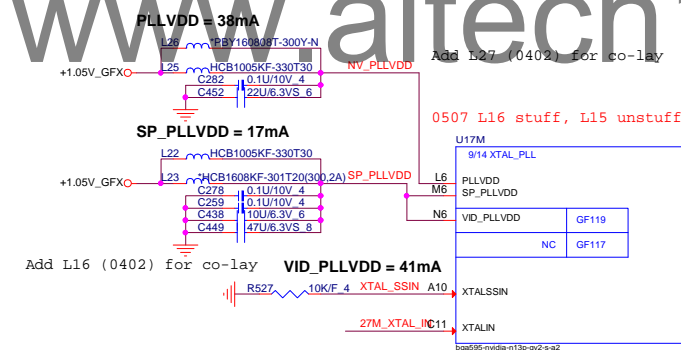


For support GC6 2.0

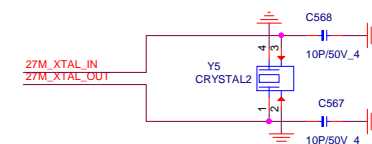


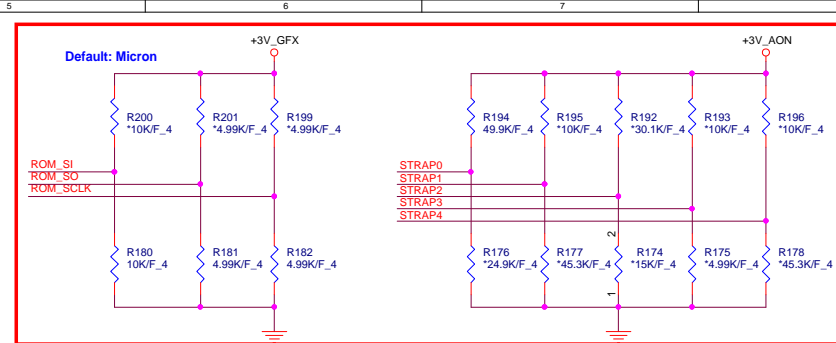


www.aitech1.ru



0310 Reserve 10K for BXTALOUT





R180 for X32	HYNIX	0101	30.1k	CS33012FB1
	Micron	0001	10k	CS31002FB2
	SAMSUNG	0000	4.99k	CS24992FB2

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	Straping	TOP B/S	QBC
0101	DDR4 256Mx32, 64bit, 8Gb	HYNIX	H5GC8H24MJR-T2C	0x5	AKD5QFUTW00	AKD5QFUTW01
0001	DDR4 256Mx32, 64bit, 8Gb	Micron	MT51U-256M32HF-60: A	0x1	AKG5LGUTL02	AKG5LGUTL03
0000	DDR4 256Mx32, 64bit, 8Gb	SAMSUNG	K4G80325FB-HC03	0x0	AKG5QGD503	AKG5QGD504

GPIO	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor
1	OUT	MEM_VDD_CTL	Memory VDD VID
2	OUT	LCD_BL_PWM	Panel Backlight PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	Reserved	--
6	OUT	FB_CLAMP_TGL_REQ	Active low FB Clamp toggle request
7	OUT	3D_VISION	3D VISION LEFT/RIGHT signal
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM_VREF_CTL	MEMORY VREF CONTROL
11	OUT	PWR_VID	GPU CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding

Memory Type	FBVDD/ FBVDDQ	Memory Density	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed CK Grade(MHz)	Memory Date Code Minimum	Status
GDDR5	1.35V/ 1.35V	256Mx16	Samsung	K4G41325FE-HC28	E-die	0x7	2500	N/A	Post production ready
			Samsung	K4G41325FC-HC03	C-die	0x3	2500	N/A	Production ready
			Hynix	H5GC4H24AJR-T2C	A-die	0x6	2500	N/A	Production ready
			Micron	EDW4032BABG-60-F	A-die	0x4	2500	N/A	Production ready
		128Mx32	Samsung	K4G41325FE-HC28	E-die	0x7	2500	N/A	Post production ready
			Samsung	K4G41325FC-HC03	C-die	0x3	2500	N/A	Production ready
			Hynix	H5GC4H24AJR-T2C	A-die	0x6	2500	N/A	Production ready
			Micron	EDW4032BABG-60-F	A-die	0x4	2500	N/A	Production ready
		256Mx32	Samsung	K4G80325FB-HC03	B-die	0x0	2500	N/A	Production ready
			Micron	MT51J256M32HF-60-A	A-die	0x1	2500	N/A	Production ready
		512Mx16	Samsung	K4G80325FB-HC03	B-die	0x0	2500	N/A	Production ready
			Micron	MT51J256M32HF-60-A	A-die	0x1	2500	N/A	Production ready

19 VMA\_DQ[63:0] VMA\_DQ[63:0]  
 19 FBA\_CMD[31:0] FBA\_CMD[31:0]  
 19 FBA\_DB[7:0] FBA\_DB[7:0]  
 19 FBA\_EDC[7:0] FBA\_EDC[7:0]

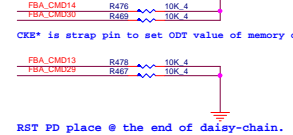
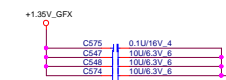
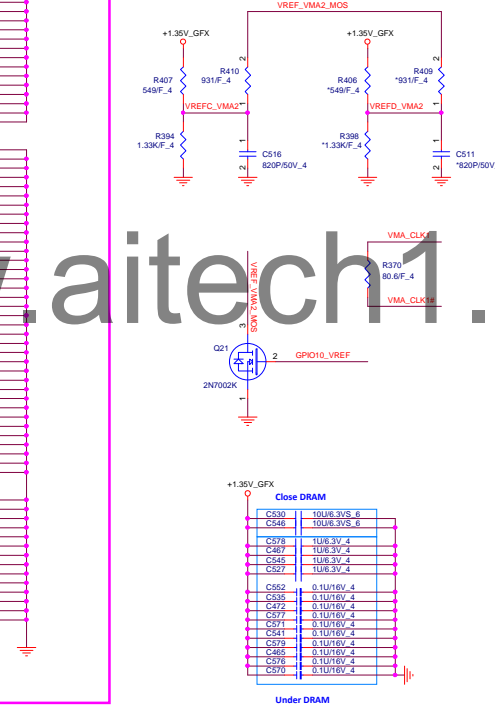
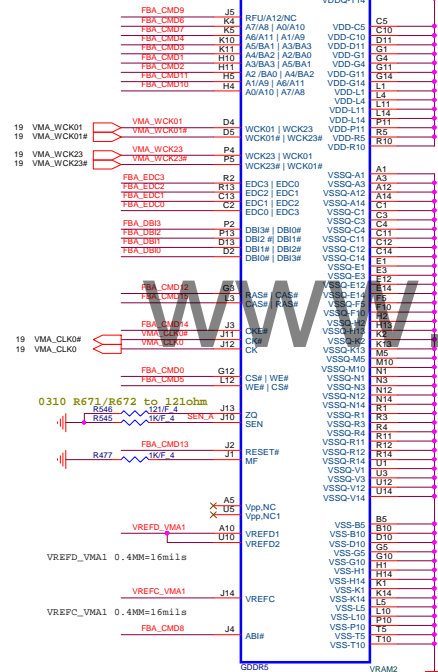
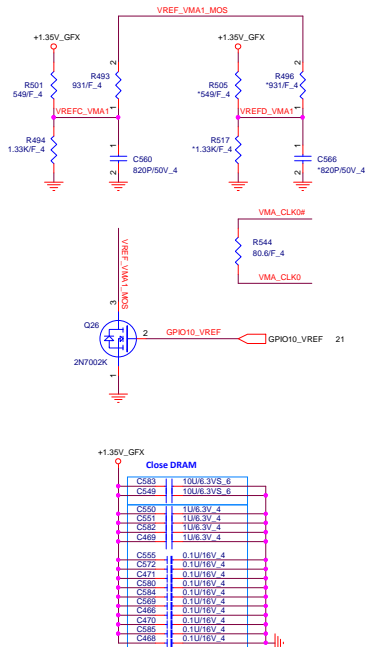
## MF=0 Non-mirrored

QD24~31

QD16~23

QD8~15

QD0~7



GDDR5 Mode H Mapping		
< 0..31 >	< 32..63 >	Memory
CHD0	CHD16	CS*
CHD1	CHD17	A3_BA3
CHD2	CHD18	A2_BA0
CHD3	CHD19	A4_BA2
CHD4	CHD20	A5_BA1
CHD5	CHD21	WE*
CHD6	CHD22	A7_A8
CHD7	CHD23	A6_A11
CHD8	CHD24	AB1*
CHD9	CHD25	A12_RFU
CHD10	CHD26	A0_A10
CHD11	CHD27	A1_A9
CHD12	CHD28	RAS*
CHD13	CHD29	RST*
CHD14	CHD30	CKE*
CHD15	CHD31	CAS*

GDDR5 CMD Mapping Table		
<0..31> <32..63> MEMORY		
12	28	RAS*
15	31	CAS*
5	21	WE*
0	16	CS*
8	24	AB1*
10	26	A0_A10
11	27	A1_A9
2	18	A2_BA0
1	17	A3_BA3
3	19	A4_BA2
4	20	A5_BA1
7	23	A6_A11
6	22	A7_A8
9	25	A12_RFU
13	29	RESET*
14	30	CKE*

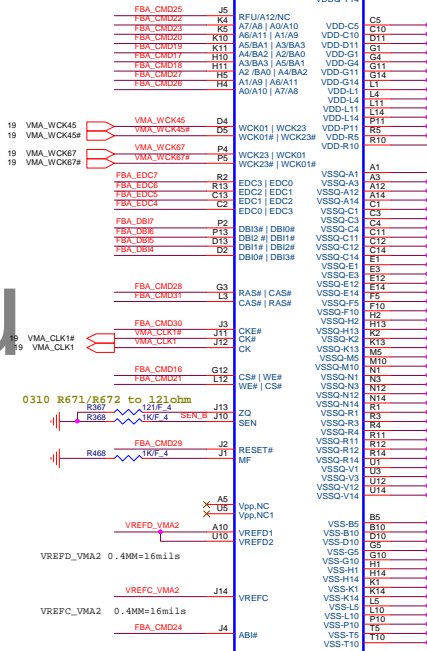
## MF=0 Non-mirrored

QD56~63

QD48~55

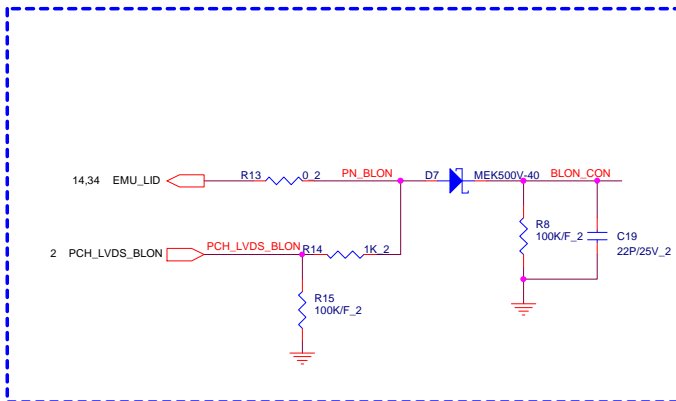
QD40~47

QD32~39

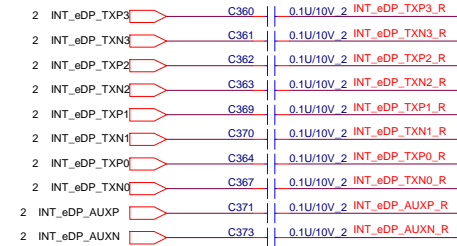
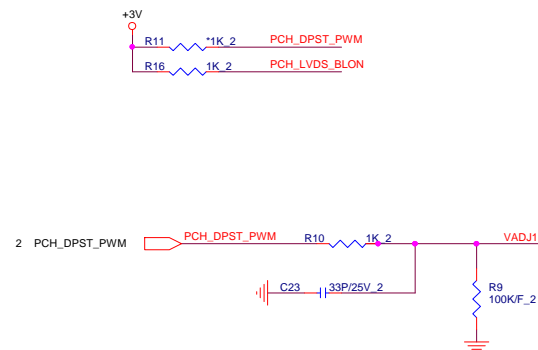
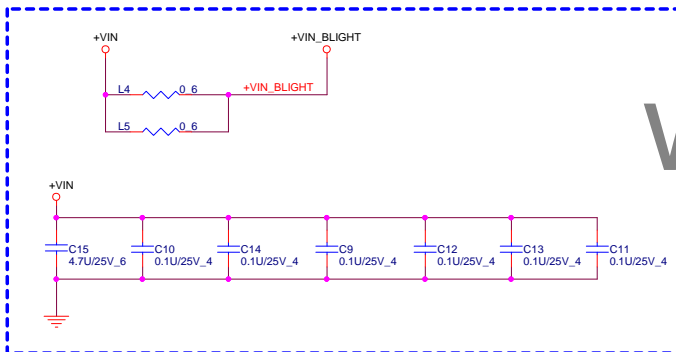




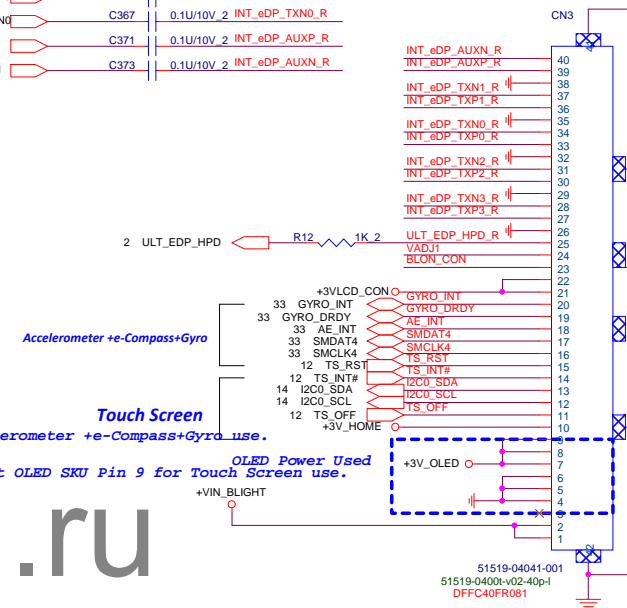
## LID Switch



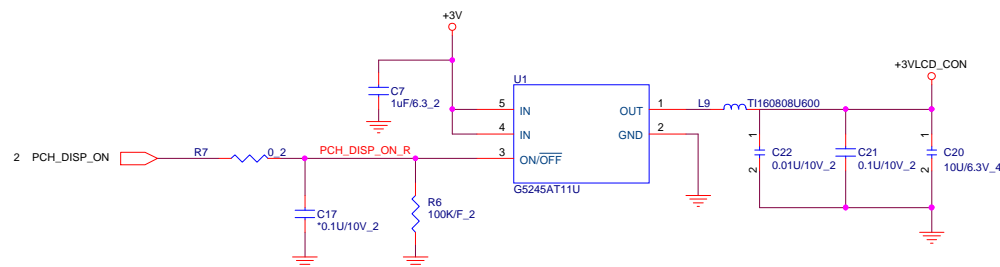
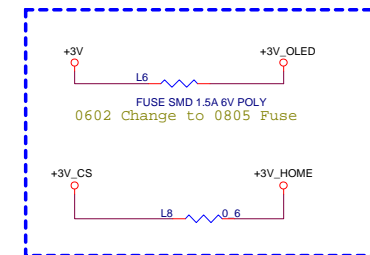
## Panel Vin Cap



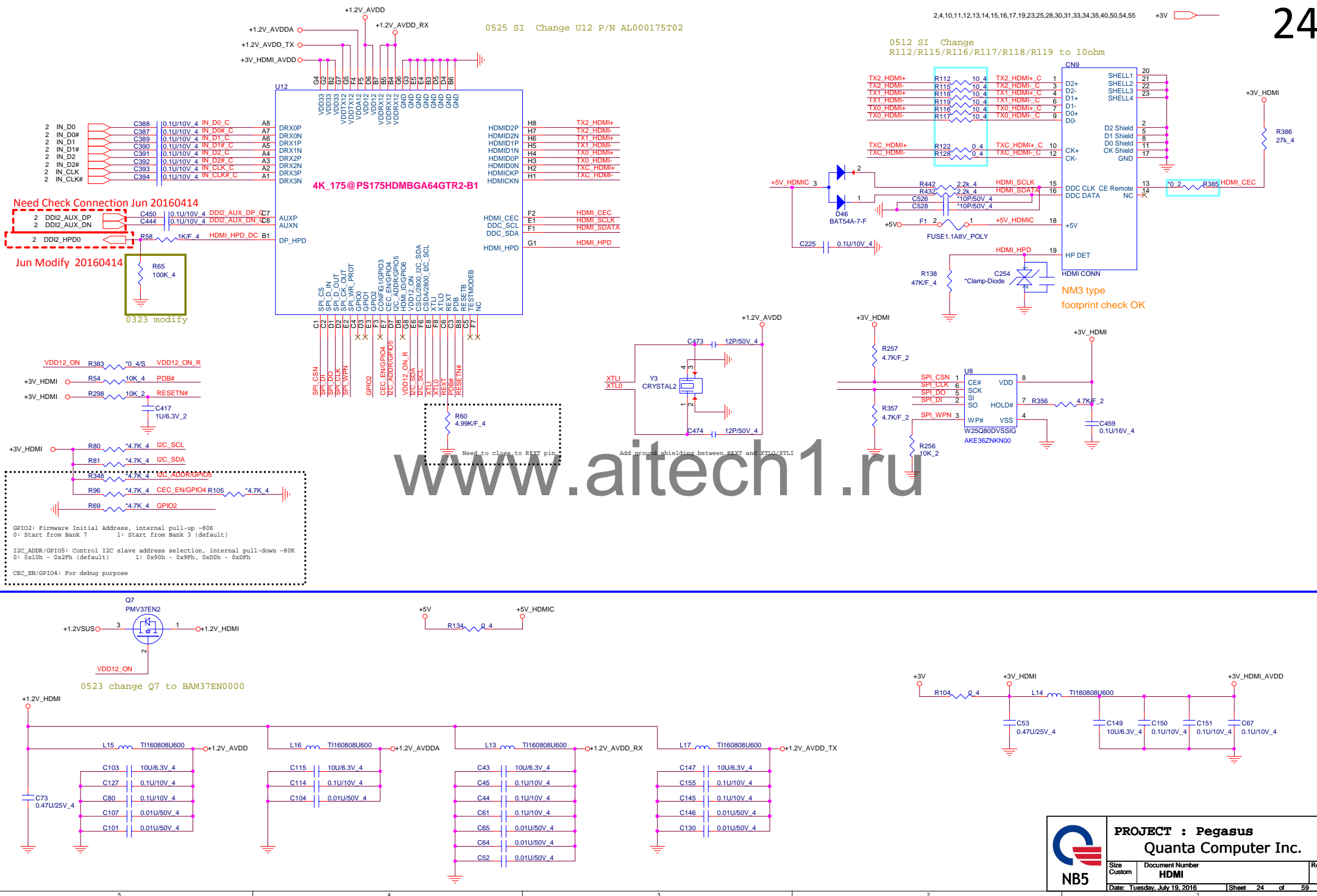
## eDP Conn.

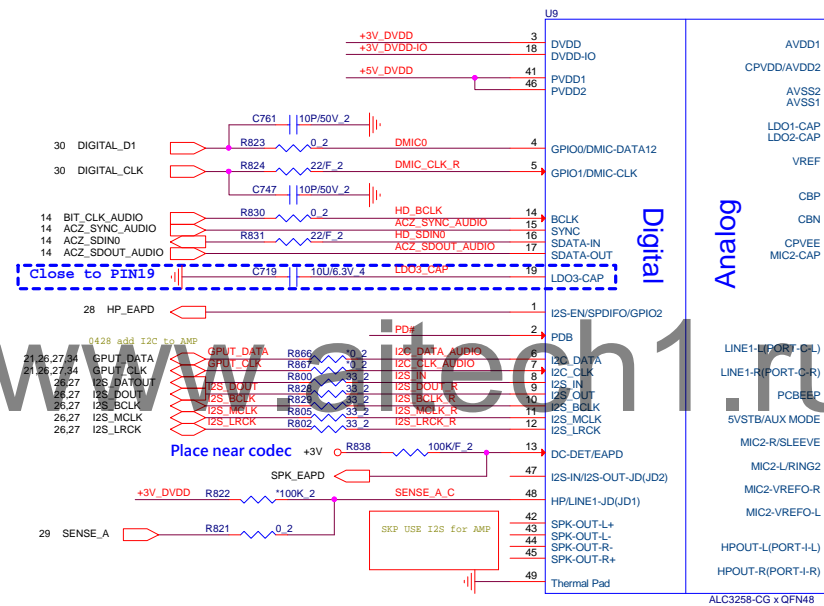
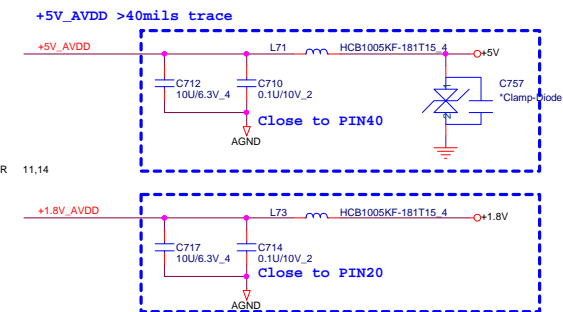
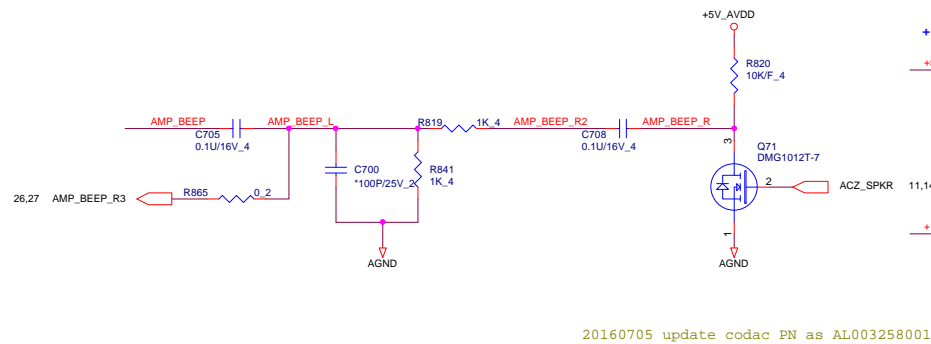
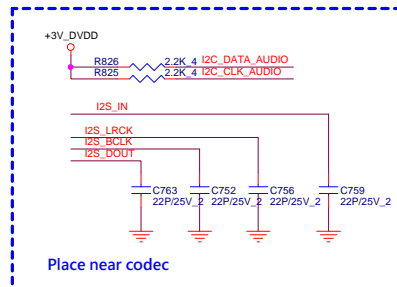
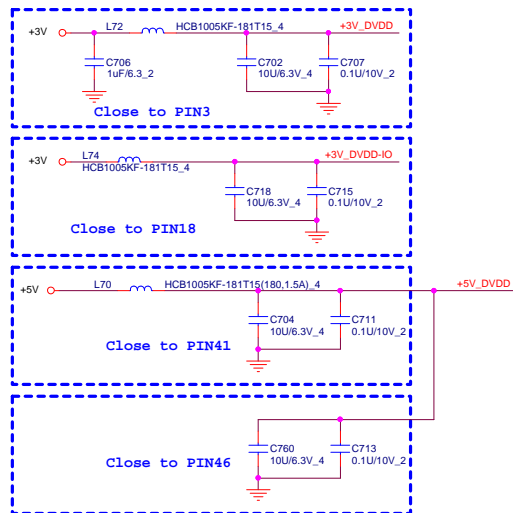


## OLED Power Used

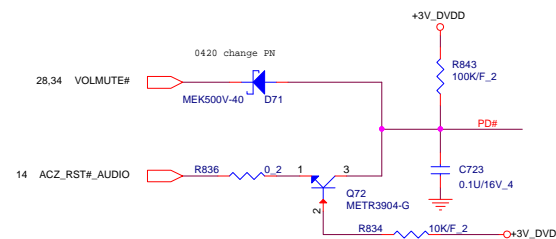


+3V 2,4,10,11,12,13,14,15,16,17,19,24,25,28,30,31,33,34,35,40,50,54,55  
+VIN 26,31,45,46,47,48,50,51,52,53,55,56,59  
+3V\_CS 33





+3V 2,4,10,11,12,13,14,15,16,17,19,23,24,28,30,31,33,34,35,40,50,54,55  
 +5V 24,28,31,54  
 +1.8V 5,54  
 +5VSS 4,26,29,37,38,40,46,47,48,49,50,51,52,54,55,56,57  
 +5VPCU 26,46,54,57



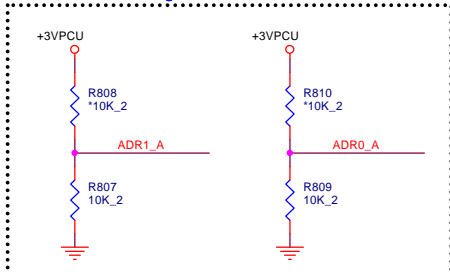
place to near or under codec



**PROJECT : X31**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Custom	<b>AUDIO CODEC ALC3258-CG</b>	
Date: Tuesday, July 19, 2016	Sheet 25 of 59	

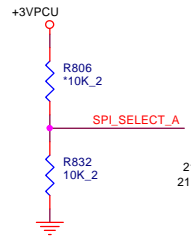
## I2C address setting



ADR0 / ADR1	
00 : 0x4C	10 : 0x4E
01 : 0x4D	11 : 0x4F

20160705 update AMP PN as AL002555T02

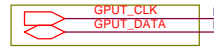
I2C/SPI select  
low:I2C  
high:SPI



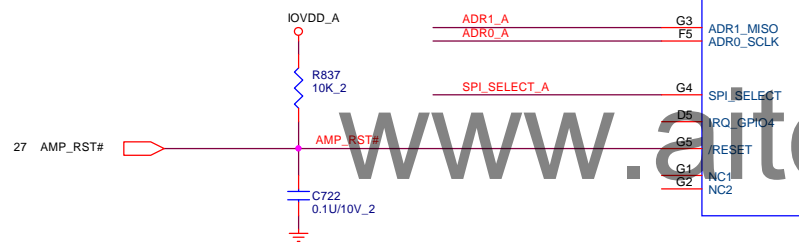
25,27 I2S\_MCLK  
25,27 I2S\_BCLK  
25,27 I2S\_LRCK  
25,27 I2S\_DOUT  
25,27 I2S\_DATAOUT



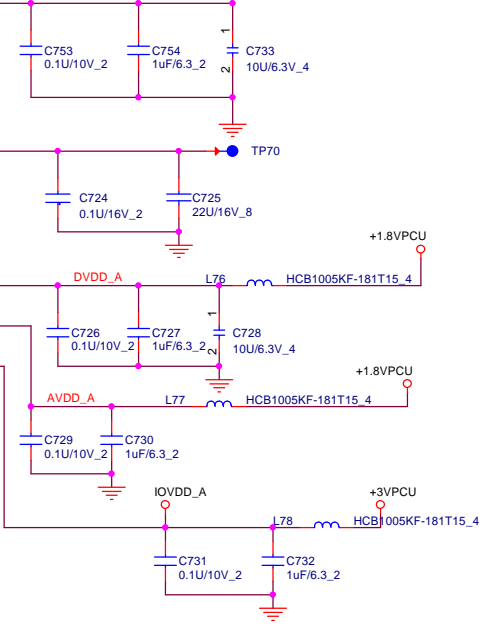
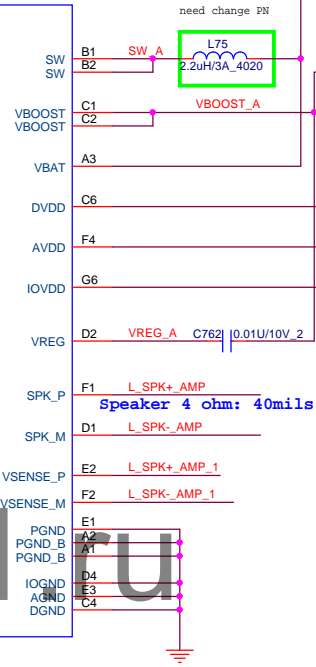
0428 for AMP



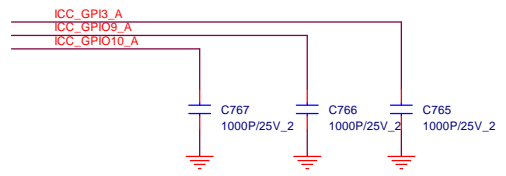
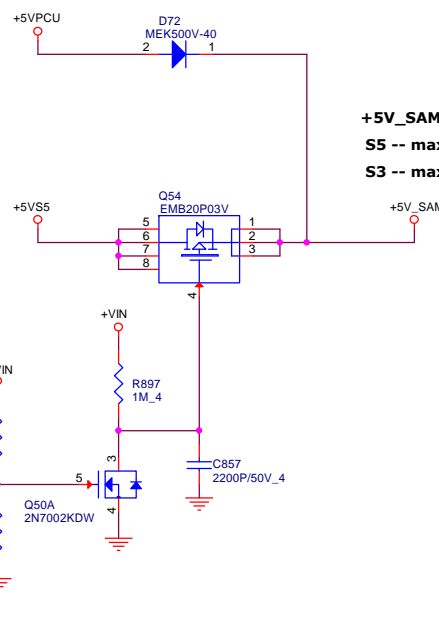
21,25,27,34 GPUT\_CLK  
21,25,27,34 GPUT\_DATA  
27 ICC\_GPIO3  
27 ICC\_GPIO9  
27 ICC\_GPIO10



TAS2555  
DSBGA 42P



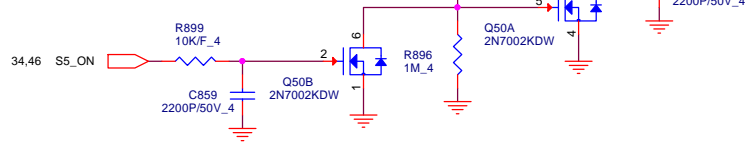
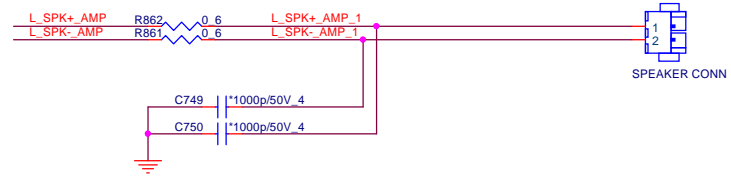
+5V\_SAMP +/- 5%  
S5 -- max output:100mA  
S3 -- max output:2A



0420 change C765/C766/C767

SPK-AMP-L

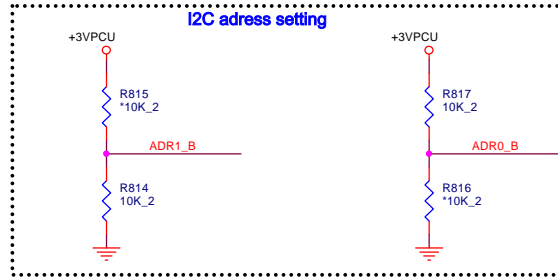
Wire White  
Wire Black



+5V\_SAMP 27  
+5VPCU 25,46,54,57  
+5VS5 4,25,29,37,38,40,46,47,48,49,50,51,52,53,55,56,59  
+VIN 23,31,45,46,47,48,50,51,52,53,55,56,59  
+3VPCU 6,13,27,29,31,32,34,37,45,46,53,58  
+5V 24,25,28,31,54  
+1.8VPCU 27,46

ADR0/ADR1	
00 : 0x4C	10 : 0X4E
01 : 0X4D	11 : 0X4F

## I2C address setting



20160705 update AMP PN as AL002555T02

U25

TAS2555  
DSBGA 42P

IN\_P  
IN\_M  
D3

MCLK\_GPIO2  
BCLK1\_GPIO1  
WCLK1\_GPIO2  
DIN1\_GPIO1  
DOUT1\_GPIO3

BCLK2\_GPIO5  
WCLK2\_GPIO6  
DIN2\_GPIO8  
DOUT2\_GPIO7

ICC\_GPIO10  
ICC\_GPIO9  
ICC\_GPIO3

ADR1\_MISO  
ADR0\_SCLK

IRQ\_GPIO4  
/RESET

NC1  
NC2

need change PN

L79

2.2uH/3A\_4020

VBOOST\_B

VBOOST

VBAT

DVDD

AVDD

IOVDD

VREG

SPK\_P

SPK\_M

VSENSE\_P

VSENSE\_M

PGND

PGND\_B

IOGND

AGND

DGND

C734

C735

C746

C736

C764

C737

C739

C738

C740

C741

C743

C744

C745

C770

C769

C768

25,26 I2S\_MCLK  
25,26 I2S\_BCLK  
25,26 I2S\_LRCK  
25,26 I2S\_DOUT  
25,26 I2S\_DATOUT

I2S\_MCLK\_B  
I2S\_BCLK\_B  
I2S\_LRCK\_B  
I2S\_DOUT\_B  
I2S\_DATOUT\_B

R851  
R852  
R854  
R853  
R855

0 2  
0 2  
0 2  
0 2  
0 2

I2C\_CLK\_AUDIO\_B  
I2C\_DATA\_AUDIO\_B

F3  
F4

SCL\_SS2  
SDA\_MOSI

0428 for AMP

GPUD\_CLK  
GPUD\_DATA

ICC\_GPIO10  
ICC\_GPIO9  
ICC\_GPIO3

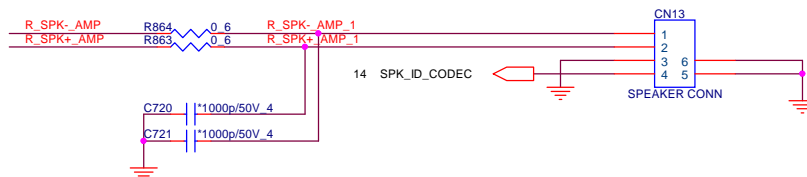
ADR1\_B  
ADR0\_B

SPI\_SELECT  
AMP\_RST#

IOVDD\_B  
AMP\_RST#

C745  
0.1u/10V\_2

## SPK-AMP-R

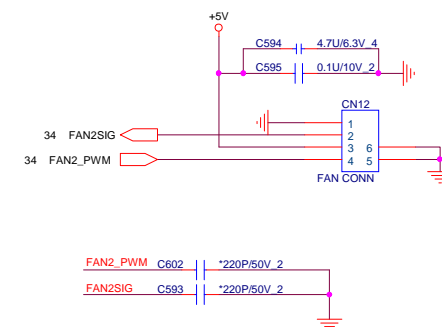
Wire Black  
Wire Red

+3VPCU 6,13,26,29,31,32,34,37,45,46,53,58  
+5V 24,25,28,31,54  
+1.8VPCU 26,46  
+5V\_SAMP 26

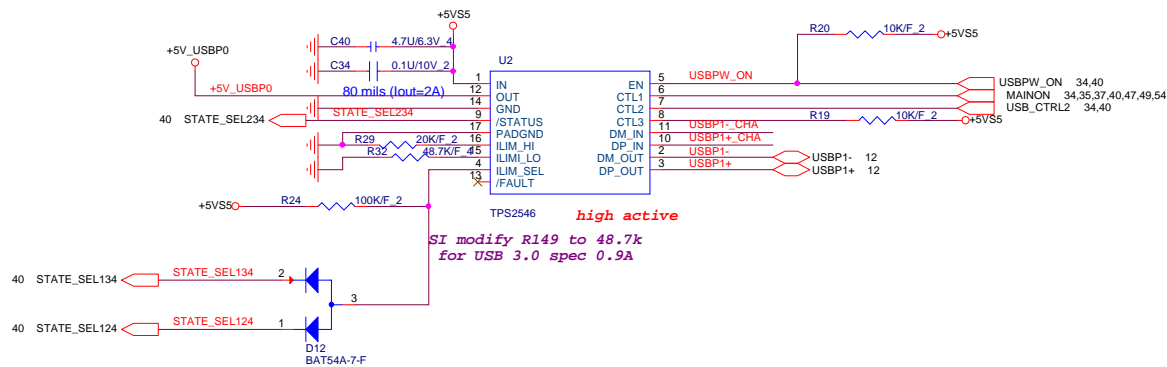


**PROJECT : X31**  
Quanta Computer Inc.

Size A3 Document Number AUDIO AMP TAS2555 Rev 1A  
Date: Tuesday, July 19, 2016 Sheet 27 of 59



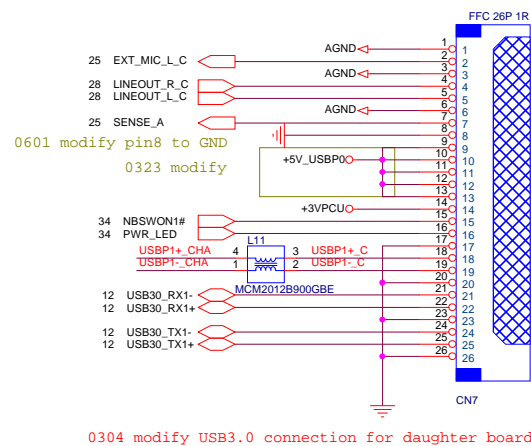




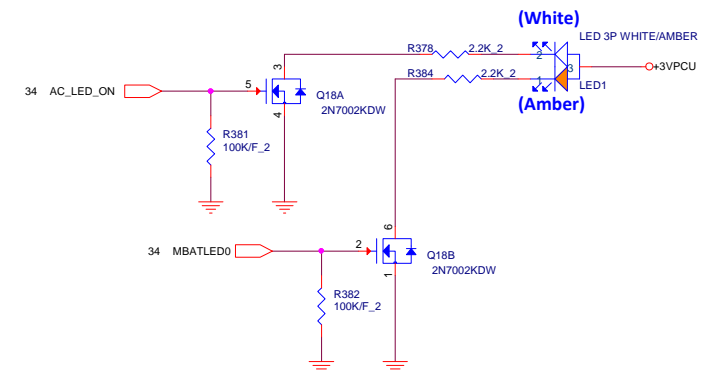
## UART for Win7 DEBUG

## Audio Combo Jack + USB3.0 Daughter Board+PW BTM

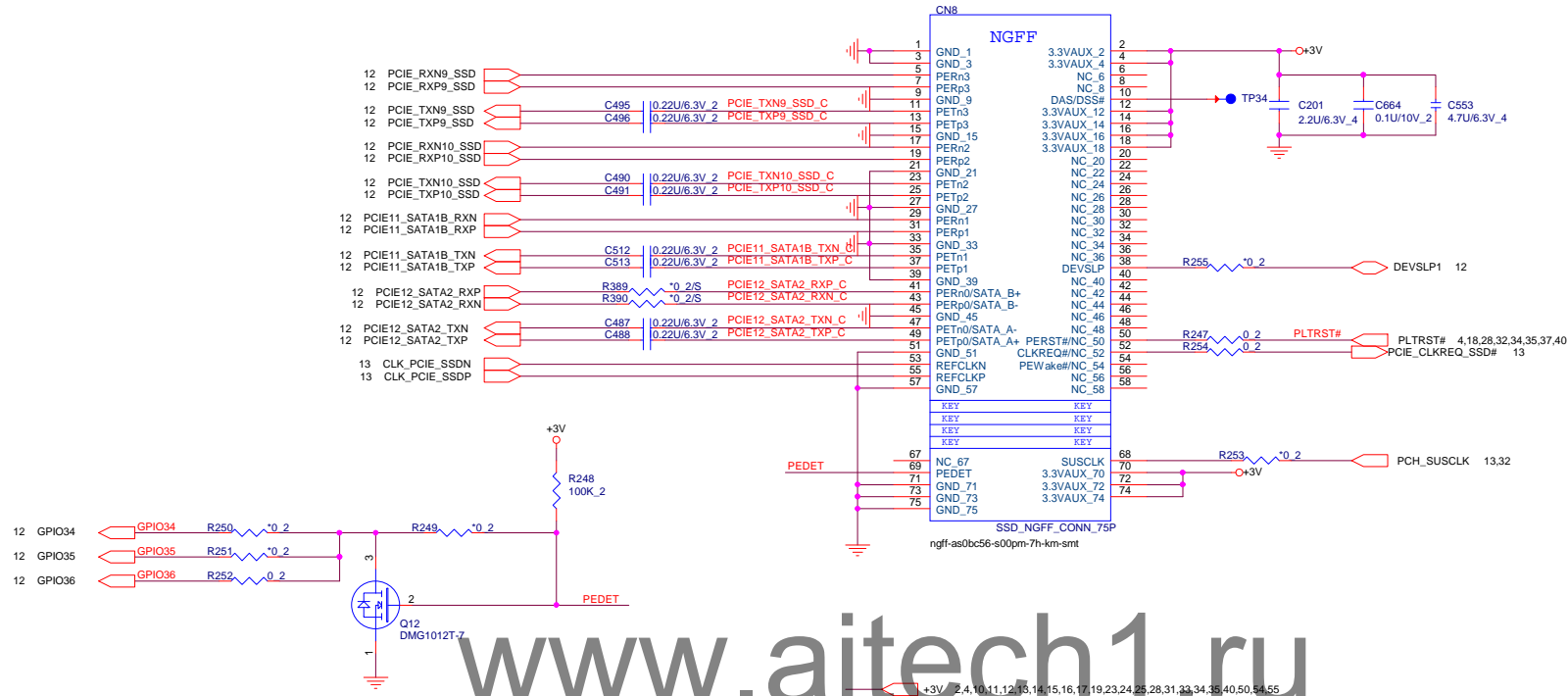
**AC\_IN / BATTERY LOW LED**



0304 modify USB3.0 connection for daughter board

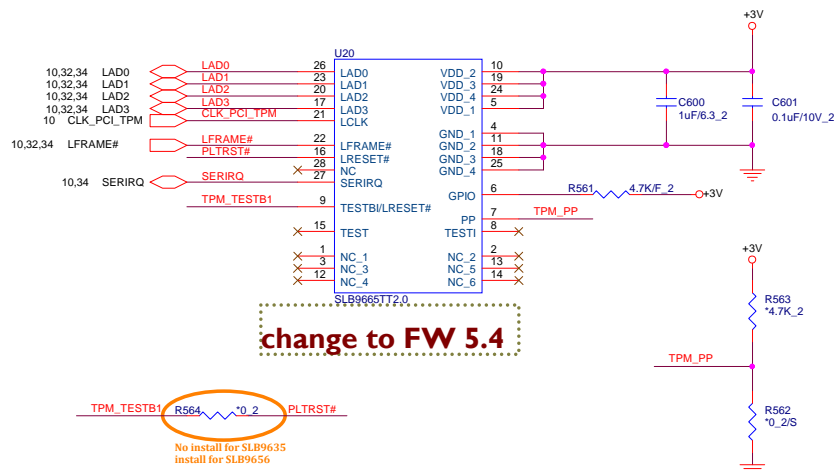


## SSD CONN

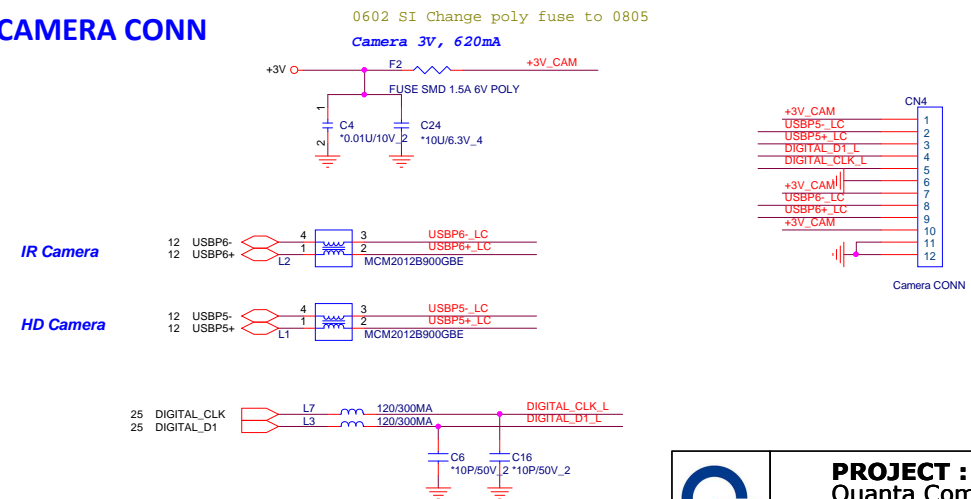
CONN: M KEY  
MODULE: N/A

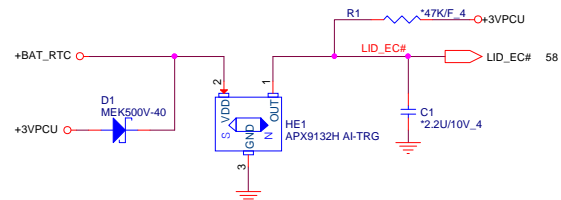
www.aitech1.ru

## TPM (2.0)

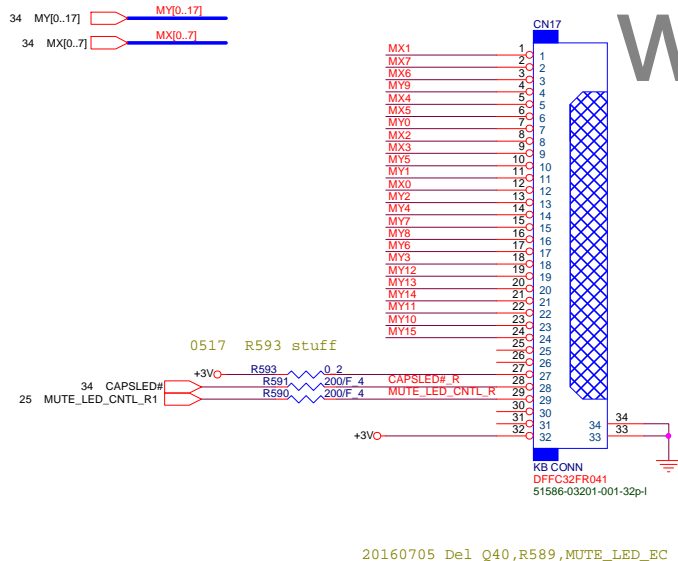


## CAMERA CONN

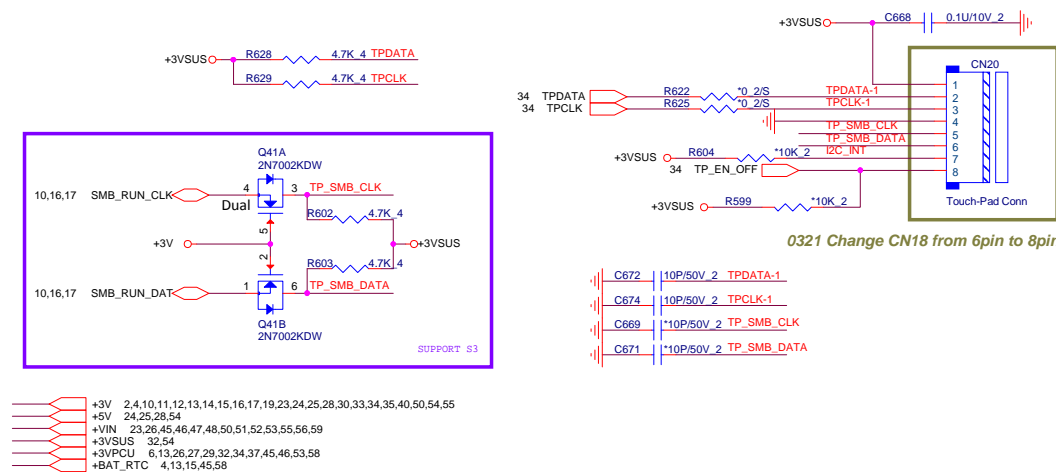




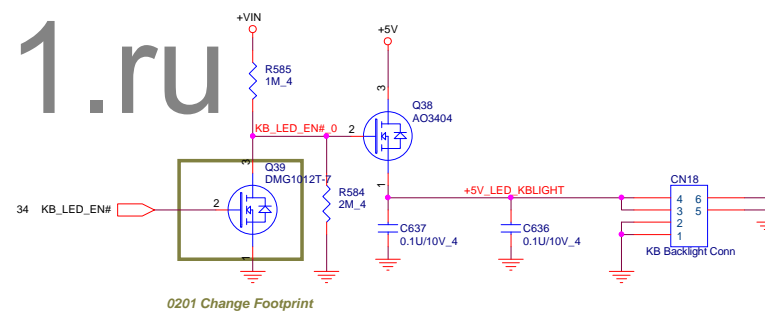
## KEYBOARD Con.

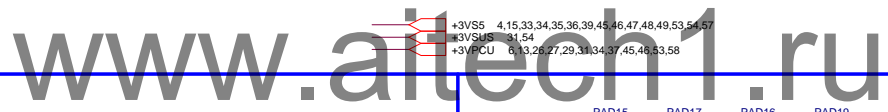


## Touch Pad Connector



## KB backlight

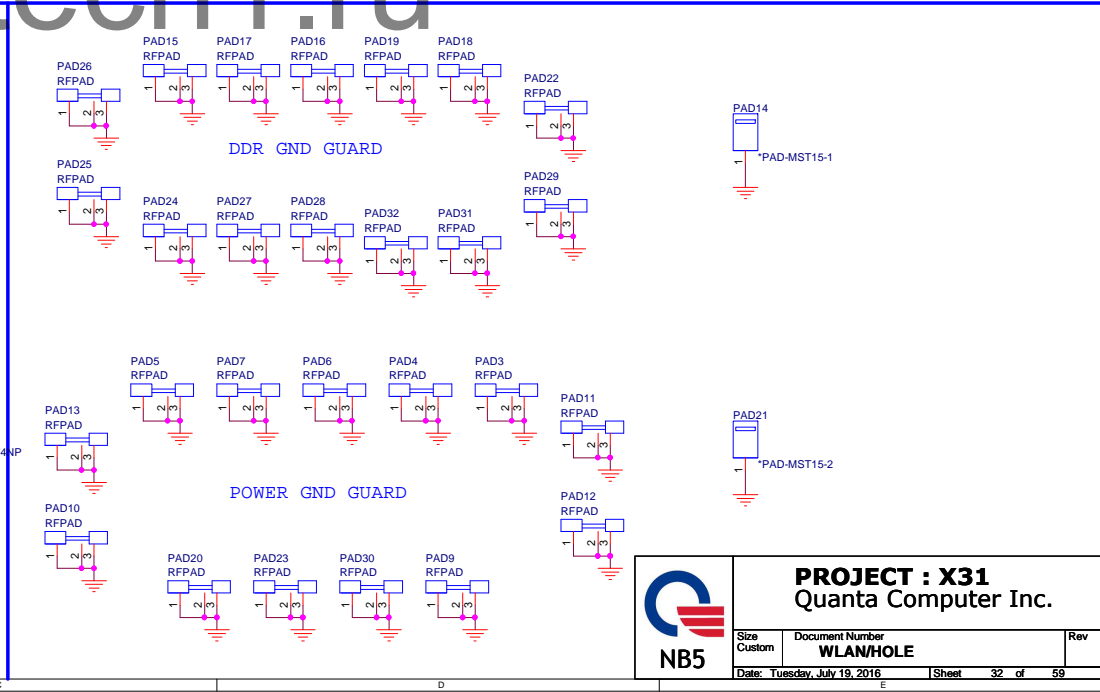




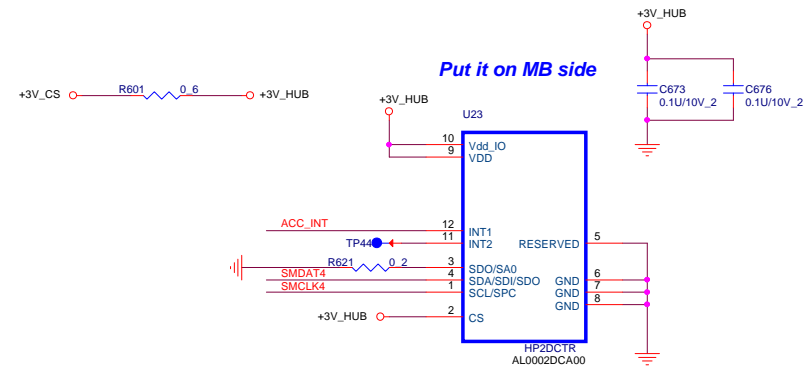
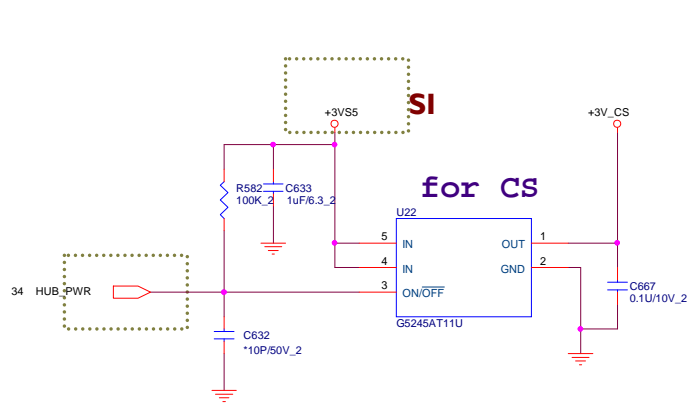
The schematic diagram illustrates the PCB layout with the following components and connections:

- CPU:** H15 (\*H-TC315IC142BC142PT), H16 (\*H-TC315IC142BC142PT), H9 (\*H-TC315IC142BC142PT), H8 (\*H-TC315IC142BC142PT), H12 (\*H-C79D79N), H11 (\*H-C79D79N).
- GPU:** H4 (\*H-C236D106P2), H6 (\*H-C276D106P2), H17 (\*H-TC315BC276D142P2), H7 (\*H-TC315IC182BC276D142P2).
- WLAN:** H5 (h-lbc217bc315d142p2).
- FAN:** H2 (\*h-lbc315ic146d106p2), H1 (\*h-lbc315ic146d106p2), H3 (\*O-MST15-A1).
- Other Components:** PAD1 (\*SPAD-S197NP), PAD8 (\*SPAD-RE157X197NP), PAD2 (\*SPAD-RE390X37), H19 (\*O-MST15-1), H10 (\*O-MST15-2), H18 (\*O-MST15-3), H20 (\*O-MST15-4), H13 (\*O-MST15-5).

The components are connected to a common ground plane, indicated by the red lines and ground symbols. The layout is organized into functional blocks, with the CPU and GPU components grouped together, and the WLAN and FAN components grouped separately.

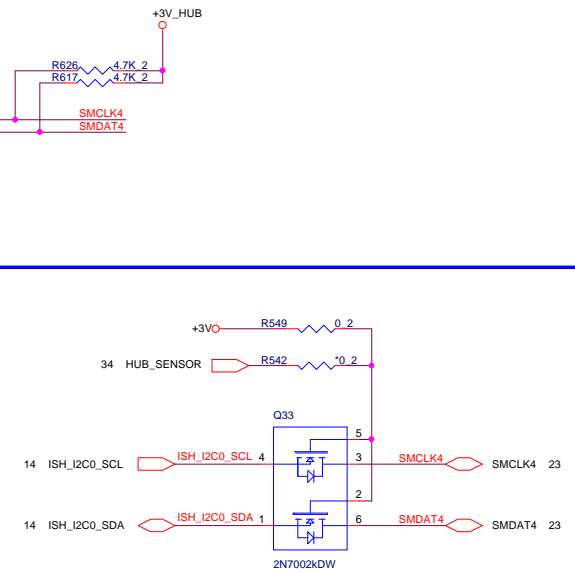
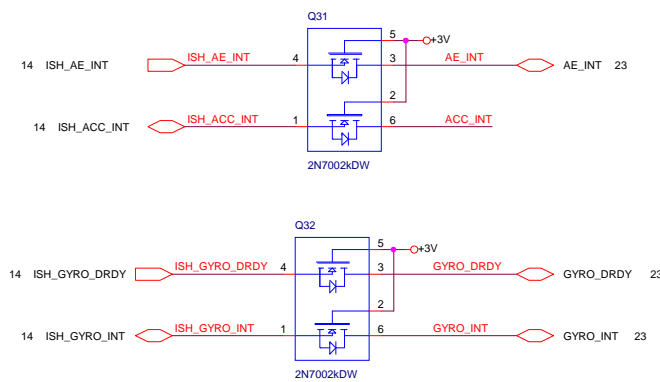


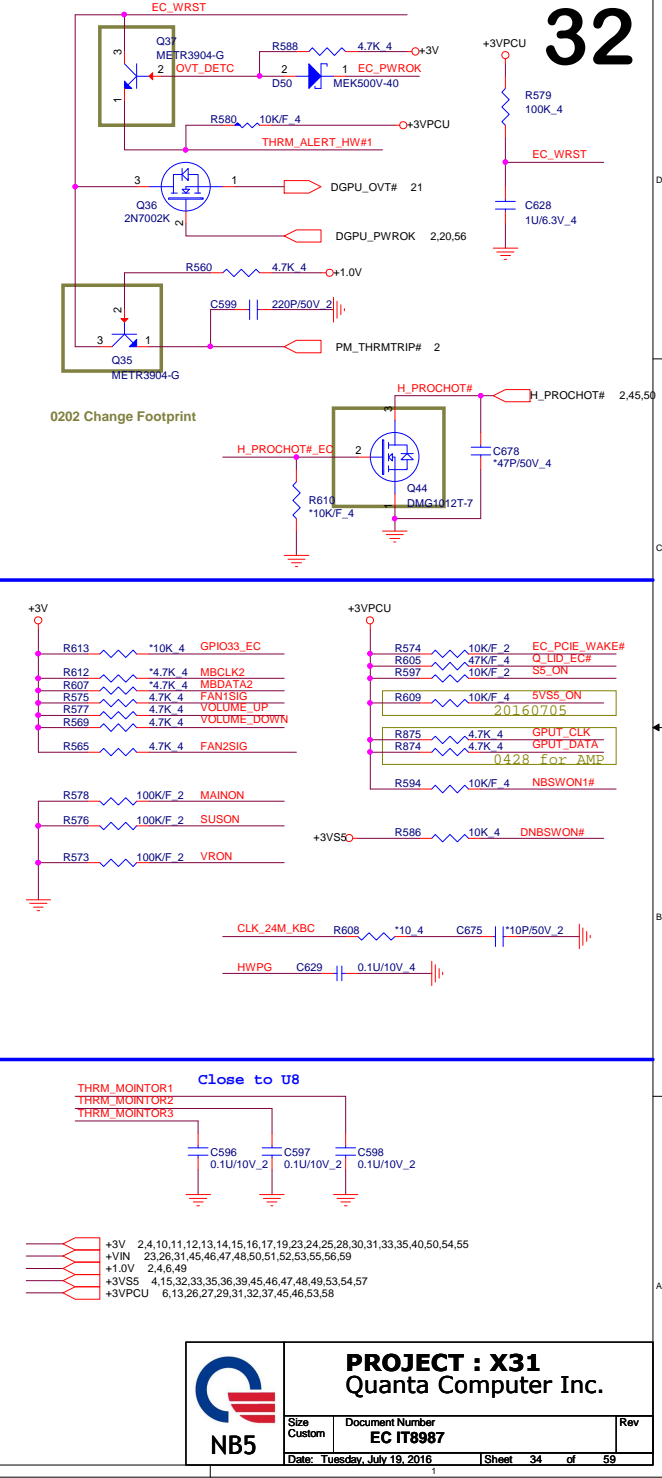
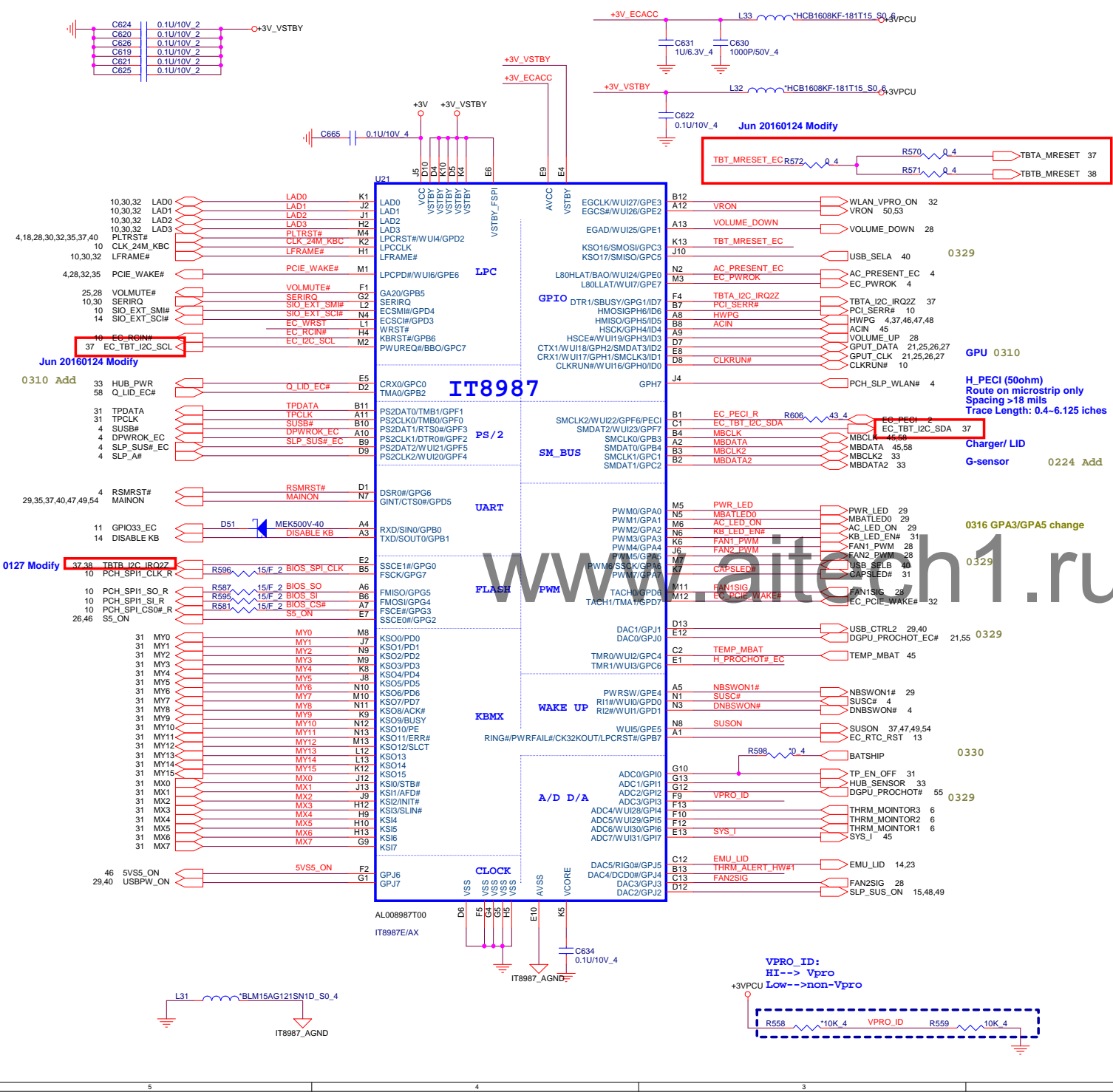
## Accelerometer Sensor



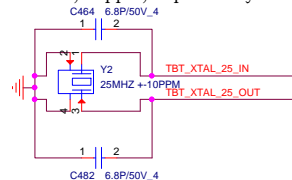
+3V 2,4,10,11,12,13,14,15,16,17,19,23,24,25,28,30,31,34,35,40,50,54,55  
 +3V5S 4,15,32,34,35,36,39,45,46,47,48,49,53,54,57  
 +3VSUS 31,32,54  
 +3V\_CS 23

www.aitech1.ru





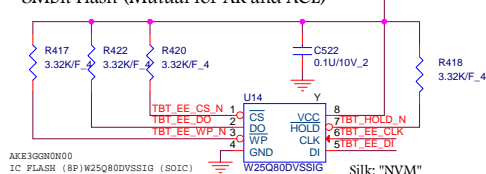
## 25MHz, 30ppm, 20pF AR Crystal



## Jun 20160124 Modify



## 8Mbit Flash (Mutual for AR and ACE)

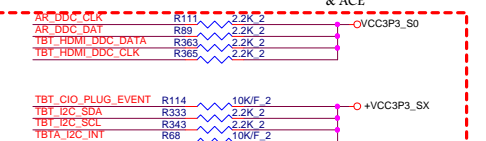


AKR30GN0N00

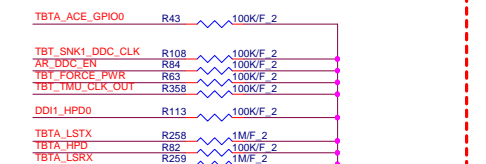
1C FLASH (8P) W25Q80DVSSIG (SOIC)

Silk: "NVM"

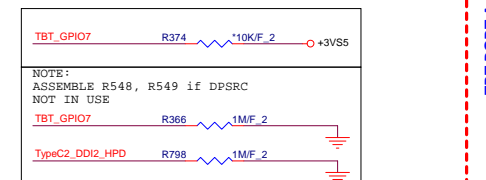
SPI/EE: AR to/from NVM &amp; ACE



## Jun Modify 20160414



## Jun Modify 20160601

TBT\_SRC\_CFG1 = 0, AUX CONNECTS TO AR  
TBT\_SRC\_CFG1 = 1, ddc CONNECTS TO AR

IF SOME OF GPIOs ARE NOT IN USE FOLLOW TABLE BELOW:

GPIO	TERMINATION	Power Rail
GPIO_0	10K PU	VCC3V3_LC
GPIO_1	10K PU	VCC3V3_LC
GPIO_2	100K PD	VCC3V3_LC
GPIO_3	100K PD	VCC3V3_LC
GPIO_4	10K PU	VCC3V3_LC
GPIO_5	10K PU	VCC3V3_LC
GPIO_6	100K PD	VCC3V3_LC
GPIO_7	100K PD	VCC3V3_LC
GPIO_8	100K PD	VCC3V3_LC
POC_GPIO_0	10K PU	VCC3V3_TBT_SX
POC_GPIO_1	10K PU	VCC3V3_TBT_SX
POC_GPIO_2	100K PD	VCC3V3_TBT_SX
POC_GPIO_3	100K PD	VCC3V3_TBT_SX
POC_GPIO_4	10K PU	VCC3V3_TBT_SX
POC_GPIO_5	10K PU	VCC3V3_TBT_SX
POC_GPIO_6	100K PD	VCC3V3_TBT_SX

## NOTE:

SNK0\_DDC\_data/clk ?connect to 2k PU only if SRC0 is connected and support HDMI (a.i HDMI or DP++ connector). Otherwise can be 100k PD.

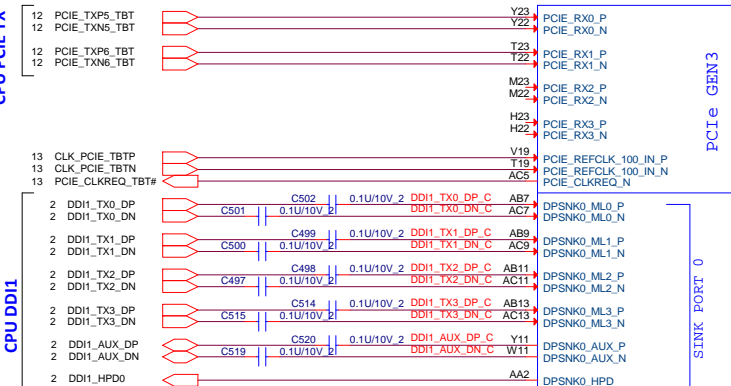
SNK1\_DDC\_data ?connect to 100k PD. If SRC0 support HDMI, connect as SNK0\_CFG1 to GPU and/or appropriate AUX/DDC demux control

SNK1\_DDC\_clk ?connect to 100k PD.

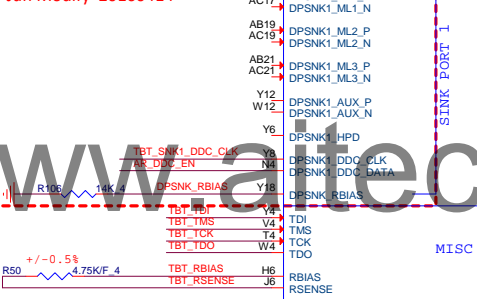
## CPU PCIe TX

## CPU DDII

## TBT PORT A



## Jun Modify 20160414



## MISC

## TBT PORTS

## POC

## DEBUG

## JTAG

## NB5

## PROJECT : X31

## Quanta Computer Inc.

## Size

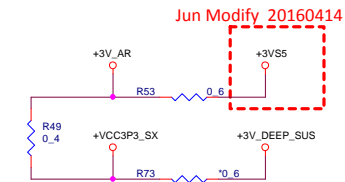
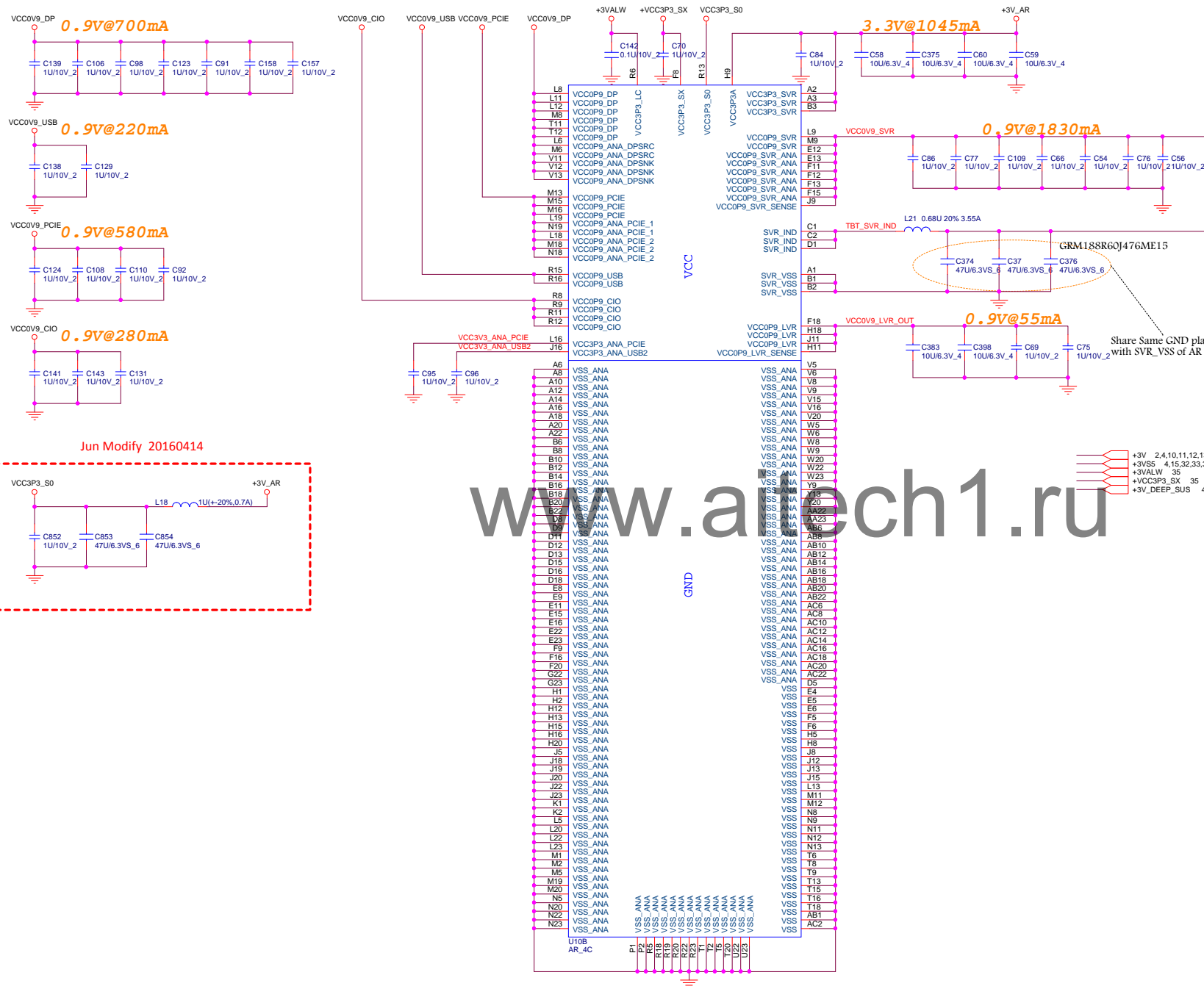
## Document Number

## Rev 1A

## Date: Tuesday, July 19, 2016

## Sheet 35 of 59





- Option 1 for wake support over TBT:
1. Connect 0Ohm to <R1> and <R3>. Keep <R2> empty.
  2. Make sure VCC3v3\_SX\_SYS can support AR maximum power consumption.
  3. Simple Bios implementation

- Option 2 for wake support over TBT:
1. Connect 0Ohm to <R1> and <R2>. Keep <R3> empty.
  2. Bios need to implement Sx entry pre-notice flow by PCIe2TBT.

No wake support at all from AR  
1. Connect 0Ohm to <R2> and <R3>. Keep <R1> empty.

Share Same GND plane  
with SVR\_VSS of AR

+3V 2,4,10,11,12,13,14,15,16,17,19,23,24,25,28,30,31,33,34,35,40,50,54,55  
 +3VS5 4,15,32,33,34,35,39,45,46,47,48,49,53,54,57  
 +3V\_ALW 35  
 +VCCP3\_SX 35  
 +3V\_DEEP\_SUS 4,10,11,12,14,15

# Port A Controller - ACE

TPS65982 (ACE) -  
USB3.1 PD

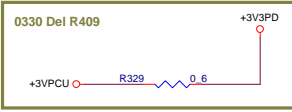
0318 Del R414 R413

PP\_EXT circuit

W = 200 mils

35

Supporting up to 60W to VBUS  
ACE configuration:  
\* SENSEP & SENSEN should be  
connected to 10mOhm resistor  
\* PP\_HV should be tied to GND.



I2C\_ADDR  
'0' - Sets ACE as Primary  
'1' - Sets ACE as Secondary

I2C1  
Connect to AR and PD2  
I2C2  
Directly to EC

Primary

Type-C USB1 Top

Type-C USB1 Bot

Jun Modify 20160414

Dual Power Role:  
BUSPOWERZ < 0.8v --> Receiving VBUS  
Power through the PP\_EXT path (Host  
Charging mode from USB)  
BUSPOWERZ > 2.4v --> Disabling system  
power from VBUS (Host providing power  
to the USB)

NOTE:  
GPIO MAPPING SUBJECT TO  
CHANGES BASED ON VENDOR  
REQUIREMENTS. PLEASE REFER TO  
DATASHEET FOR MORE DETAILS.



PROJECT : X31  
Quanta Computer Inc.

Size	Document Number	Rev
	AR - TBT (USB2 & DP Part)	1A
Date: Tuesday, July 19, 2016	Sheet 37 of 59	

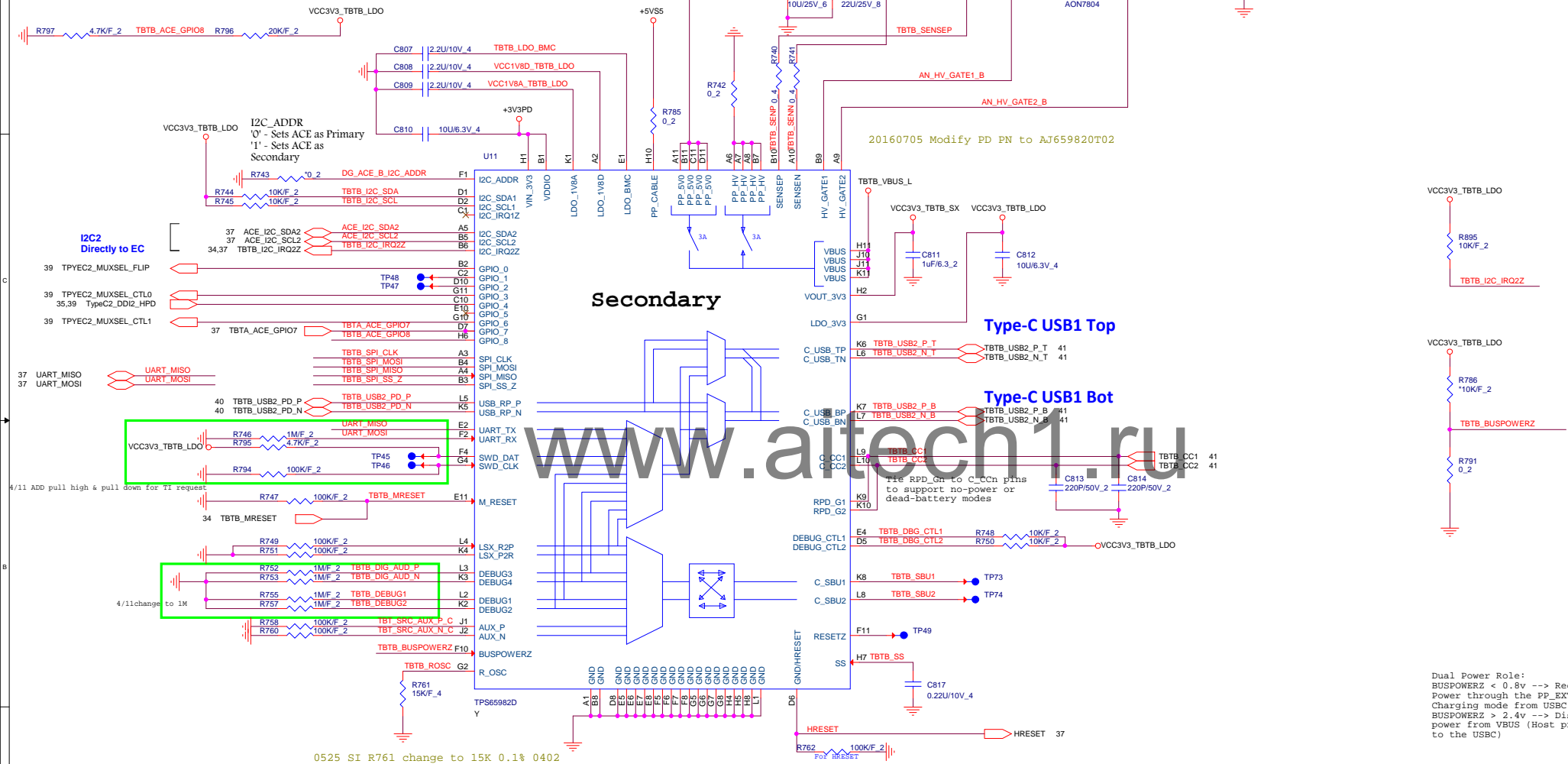
### Port B Controller - ACE

TPS65982 (ACE) - USB3.1  
PD

PP\_EXT

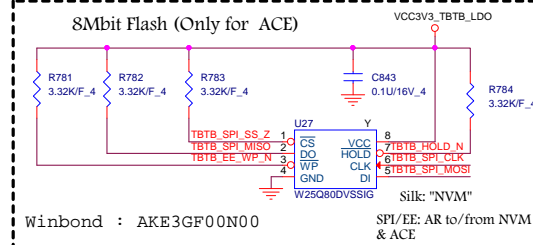
Supporting up to 60W to VBUS  
ACE configuration:  
\* SENSEP & SENSEN should be  
connected to 10mOhm resistor  
\* PP\_HV should be tied to GND.

TBTB\_VBUS\_L  
W = 200 mils



```
Dual Power Role:
BUSPOWERZ < 0.8v --> Receiving VBUS
Power through the PP_EXT path (Host
Charging mode from USB)
BUSPOWERZ > 2.4v --> Disabling system
power from VBUS (Host providing power
to the USB)
```

## 8Mbit Flash (Only for ACE)



NOTE:  
GPIO MAPPING SUBJECT TO  
CHANGES BASED ON VENDOR  
REQUIREMENTS. PLEASE REFER TO  
DATASHEET FOR MORE DETAILS.



**PROJECT : X31**  
Quanta Computer Inc.

Size	Document Number <b>AR - TBT (USB2 &amp; DP Part)</b>	Rev 1A
Date: Tuesday, July 19, 2016	Sheet 38 of	59

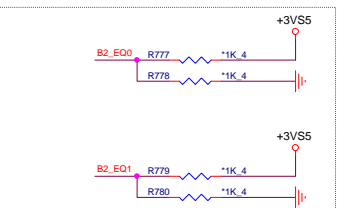
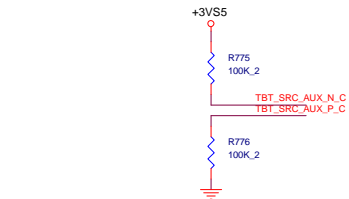
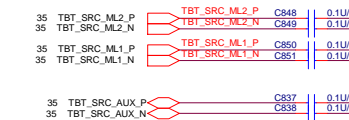
## 4 Level Input:

- L: Option1 Tie 1Kohm 5% to GND  
Option2 Directly tie to GND  
R: Tie 20kohm 5% to GND  
F: Float(leave pin open)  
1: Option1 Tie 1Kohm 5% to Vcc  
Option2 Directly tie to Vcc

## DisplayPort Source

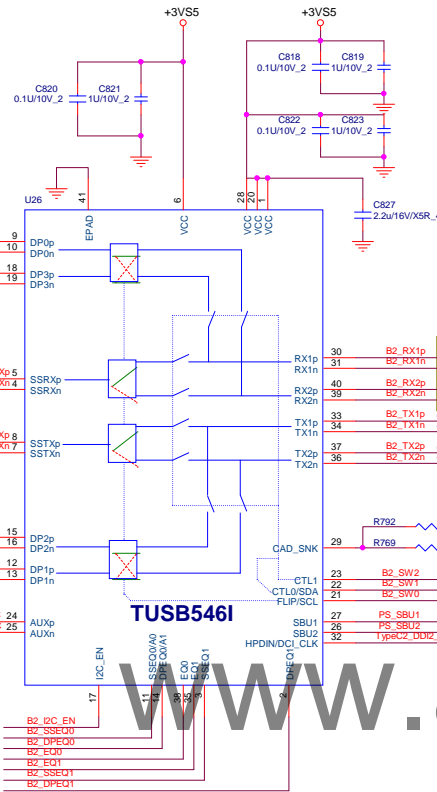


## USB3.0 HOST



EQ0, EQ1 : USB receiver equalizer gain  
for downstream facing RX1 & RX2  
F, F(Default)

I2C Programming or pin strap programming select.  
I2C is only disable when this pin is '0'  
0 : Pin Strap(I2C disable)(Default)  
1 : TI test mode(I2C enable at 3.3V)  
F : I2C enabled at 1.8V  
1 : I2C enabled at 3.3V



CTL1	CTL0	FLIP	TUSB546 Mode Selection
L	L	L	Chip Power Down
L	L	H	Chip Power Down
L	H	L	One Port USB 3.1 - No Flip
L	H	H	One Port USB 3.1 - With Flip
H	L	L	4 Lane DP - No Flip
H	L	H	4 Lane DP - With Flip
H	H	L	One Port USB 3.1 + 2 Lane DP - No Flip
H	H	H	One Port USB 3.1 + 2 Lane DP - With Flip

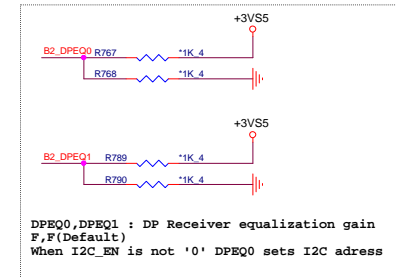
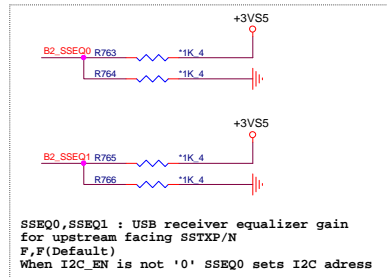
## TUSB546 Pin Control Mode

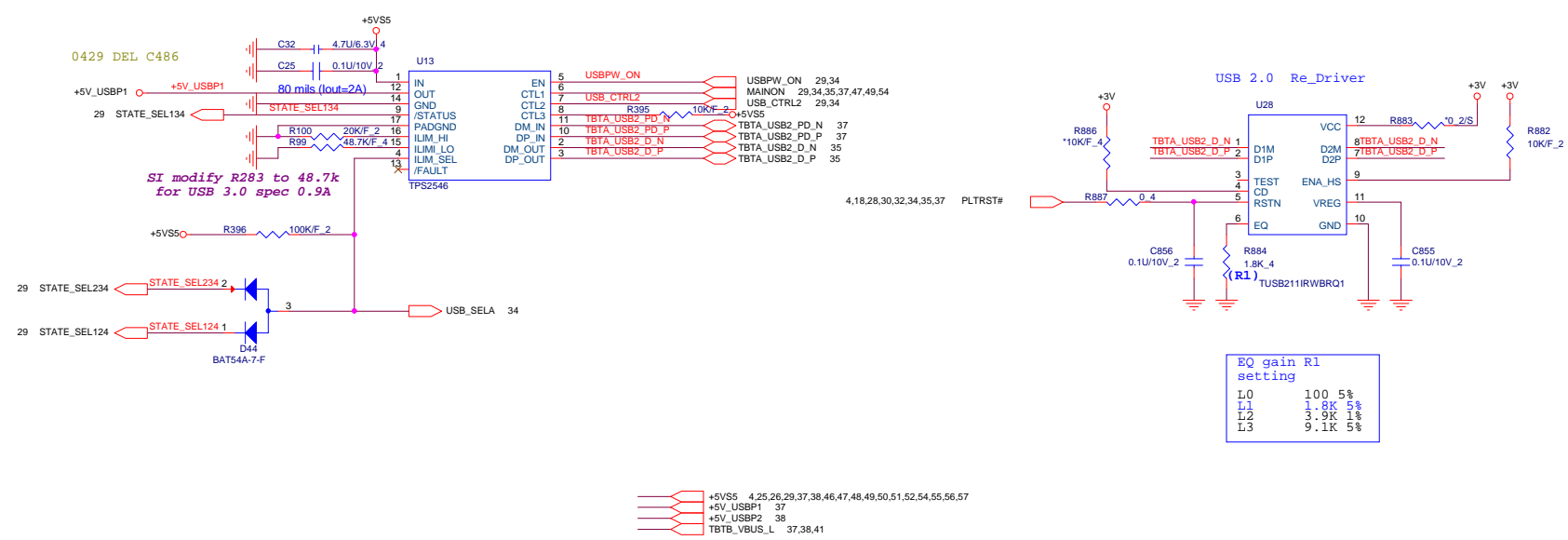
CTL1	FLIP	AUX Select
H	L	AUXP->SBU1, AUXN->SBU2
H	H	AUXP->SBU2, AUXN->SBU1
L>2ms	X	One Port USB 3.1 - No Flip

## AUX Pin Control Mode

Table 8-7 TUSB546 Receiver Equalization GPIO Control

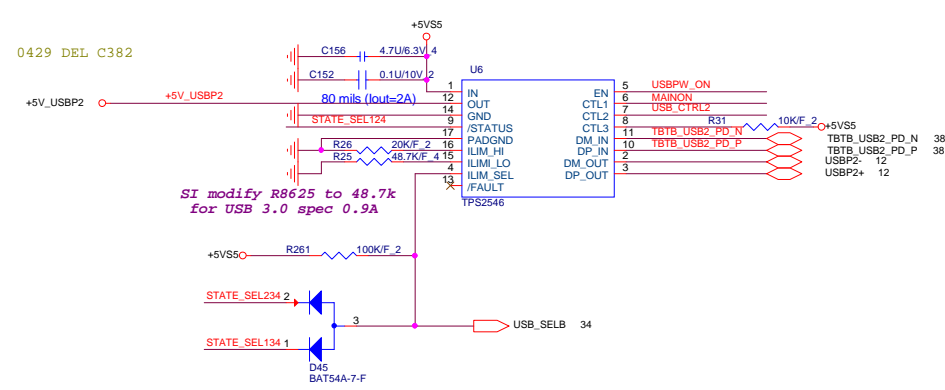
USB3.1 Downstream Facing Ports			USB 3.1 Upstream Facing Ports			All DisplayPort Lanes		
EQ1 pin Level	EQ0 pin Level	EQ GAIN @2.5GHz (dB)	SSEQ1 pin Level	SSEQ0 pin Level	EQ GAIN @2.5GHz (dB)	DPEQ1 pin Level	DPEQ0 pin Level	EQ GAIN @2.5GHz (dB)
0	0	0	0	0	0	0	0	0
0	R	1	0	R	1	0	R	1
0	F	2	0	F	2	0	F	2
0	1	3	0	1	3	0	1	3
R	0	4	R	0	4	R	0	4
R	R	5	R	R	5	R	R	5
R	F	6	R	F	6	R	F	6
R	1	7	R	1	7	R	1	7
F	0	8	F	0	8	F	0	8
F	R	9	F	R	9	F	R	9
F	1	10	F	1	10	F	1	10
F	F	11	F	F	11	F	F	11
1	0	12	1	0	12	1	0	12
1	R	13	1	R	13	1	R	13
1	F	14	1	F	14	1	F	14
1	1	15	1	1	15	1	1	15



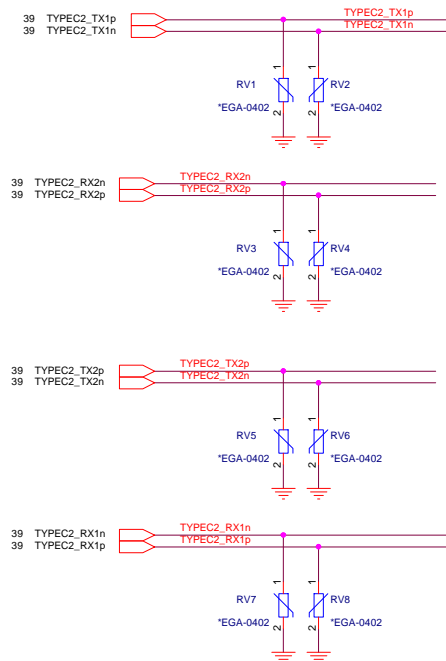


PortB Support BC1.2

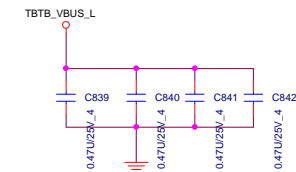
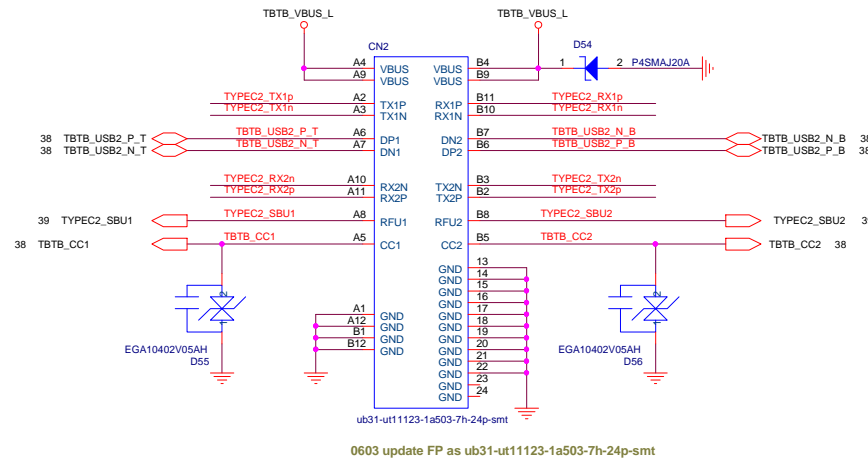
www.aitech1.ru



# Type C2\_HSIO\_ESD

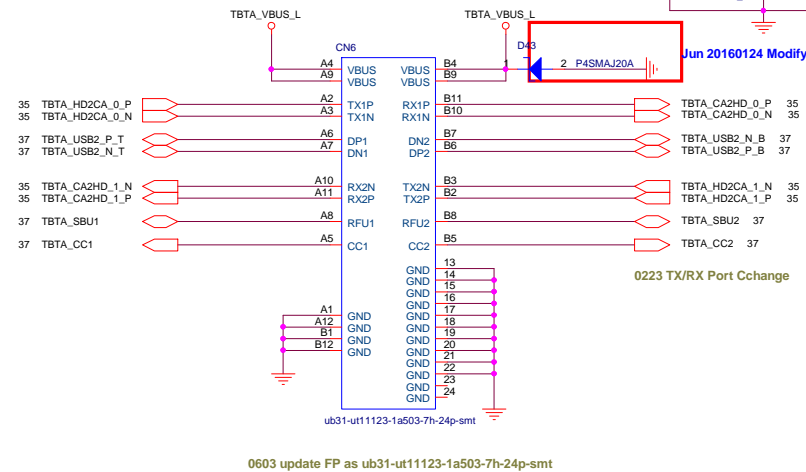


## USB Type-C Port B



www.aitech1.ru

USB Type-C Port A CN6 位置在HDMI CN上面



0604 update PN as BC0101B1Z01

0503 update FP as d-0\_62x0\_32-0\_32h

TBTA_USB2_P_T	1	2	ESD101-B1-02ELS
TBTA_USB2_N_T	1	2	ESD101-B1-02ELS
TBTA_USB2_P_B	1	2	ESD101-B1-02ELS
TBTA_USB2_N_B	1	2	ESD101-B1-02ELS
TBTA_CC1	1	2	ESD101-B1-02ELS
TBTA_CC2	1	2	ESD101-B1-02ELS
TBTA_SBU1	1	2	ESD101-B1-02ELS
TBTA_SBU2	1	2	ESD101-B1-02ELS

TBTA_HD2CA_0_P	1	2	ESD101-B1-02ELS
TBTA_HD2CA_0_N	1	2	ESD101-B1-02ELS
TBTA_CA2HD_0_P	1	2	ESD101-B1-02ELS
TBTA_CA2HD_0_N	1	2	ESD101-B1-02ELS
TBTA_CA2HD_1_P	1	2	ESD101-B1-02ELS
TBTA_CA2HD_1_N	1	2	ESD101-B1-02ELS
TBTA_HD2CA_1_N	1	2	ESD101-B1-02ELS
TBTA_HD2CA_1_P	1	2	ESD101-B1-02ELS

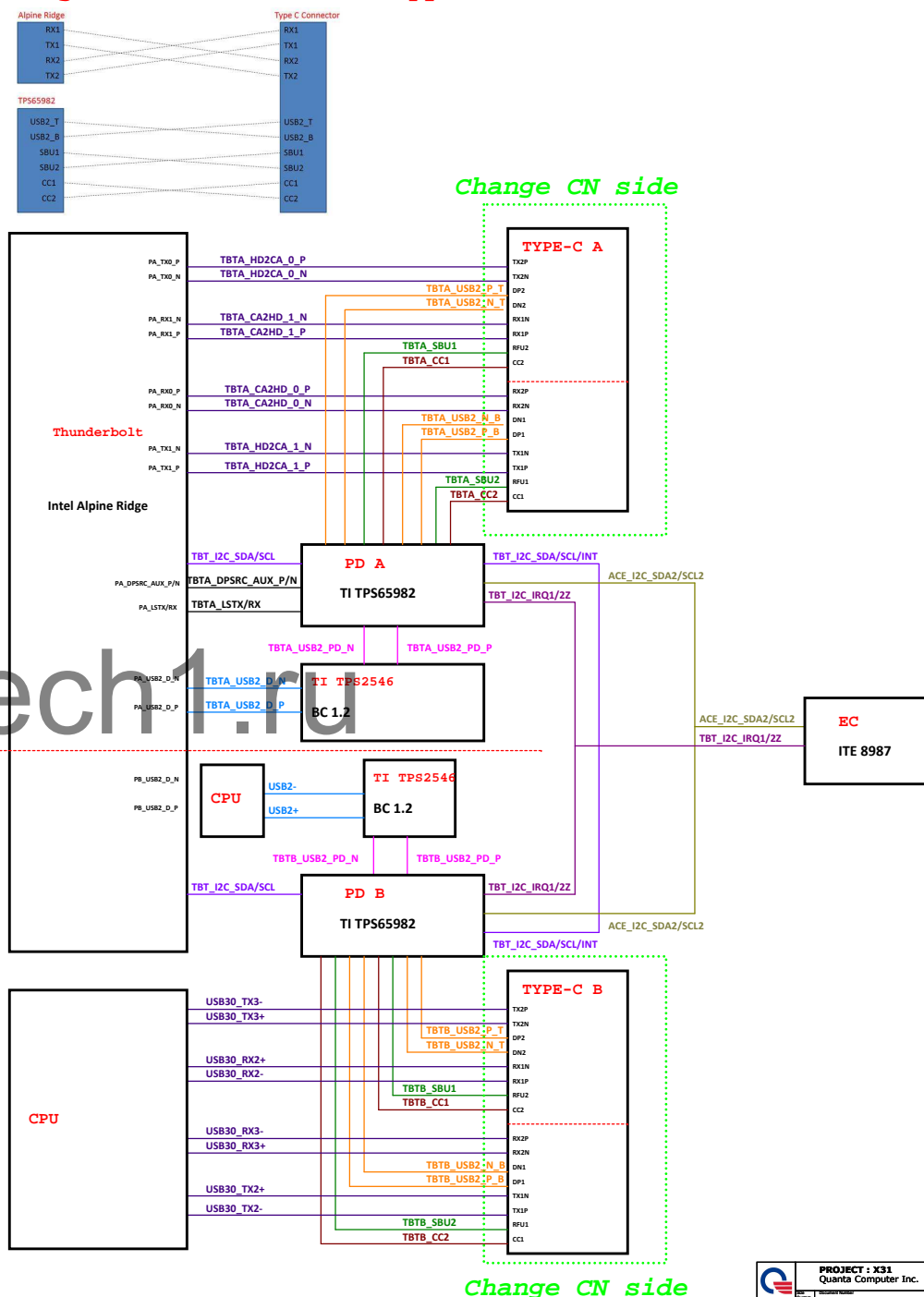
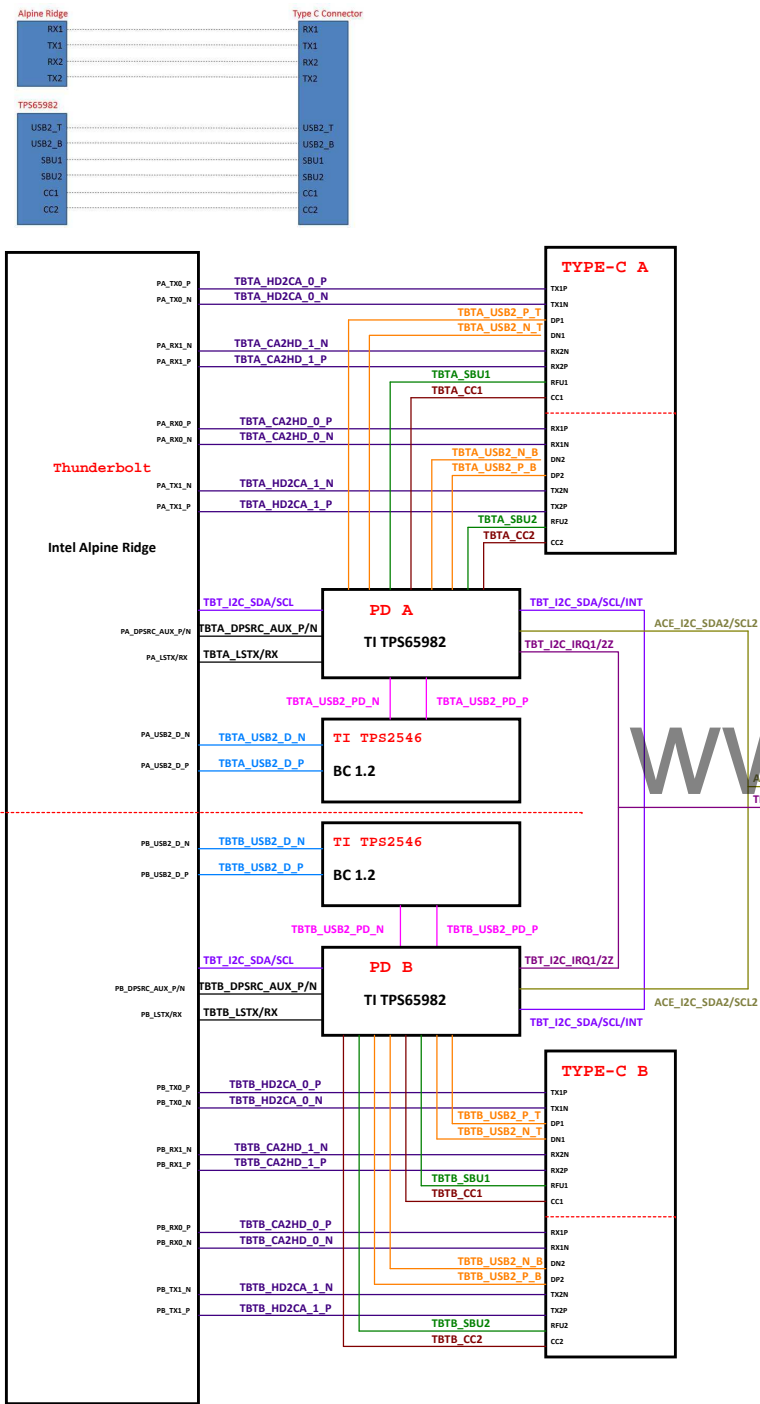


**PROJECT : X31**  
**Quanta Computer Inc.**

Size	Document Number	Rev
NB5	AR - TBT (USB2 & DP Part)	1A
Date: Tuesday, July 19, 2016	Sheet 41 of 59	

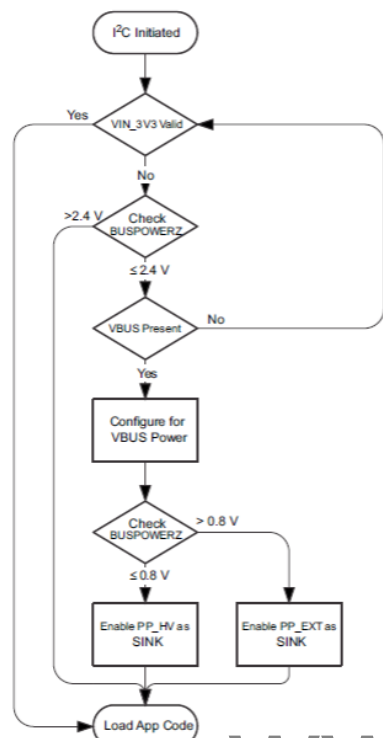
Keep the same Typc-C CN as the same as Intel AR CRB Board

Change CIO connection in Type-C Connector side





## Dead Battery Block



## USB Type-C Connector – Pinout and Alignment



Receptacle (Front View)

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1-	VBUS	CC1	D+	D-	SBU1	VBUS	RX2-	RX2+	GND
GND	RX1+	RX1-	VBUS	SBU2	D-	D+	CC2	VBUS	TX2-	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

USB3.0                      USB2.0                      USB3.0



Normal Plug

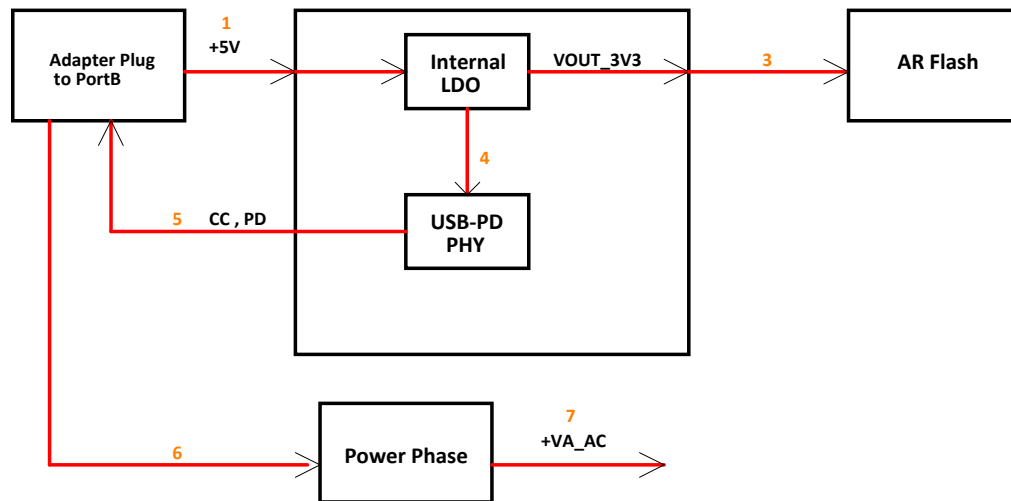


Reverse Plug

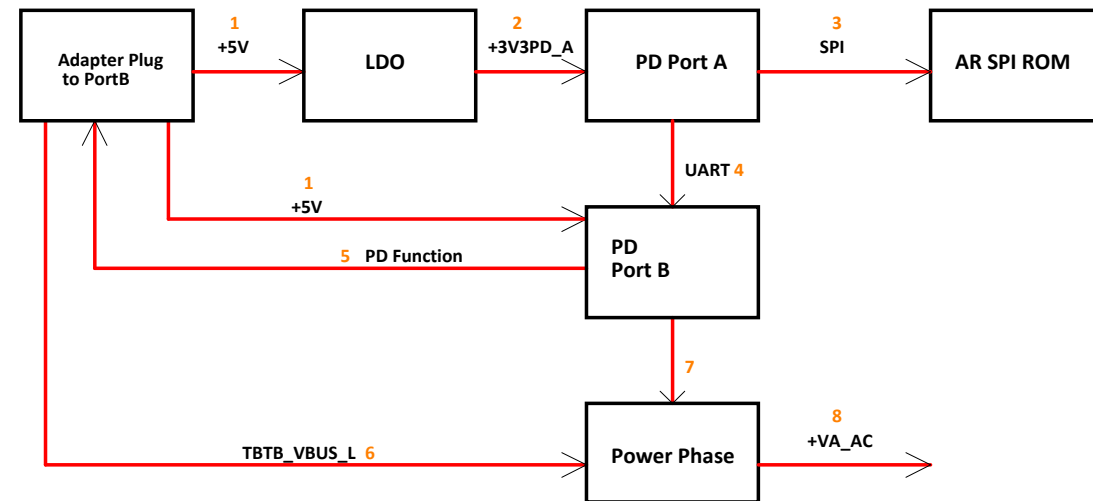


A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
GND	RX2+	RX2-	VBUS	SBU1	D-	D+	CC	VBUS	TX1-	TX1+	GND
GND	TX2+	TX2-	VBUS	VCONN			SBU2	VBUS	RX1-	RX1+	GND
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12

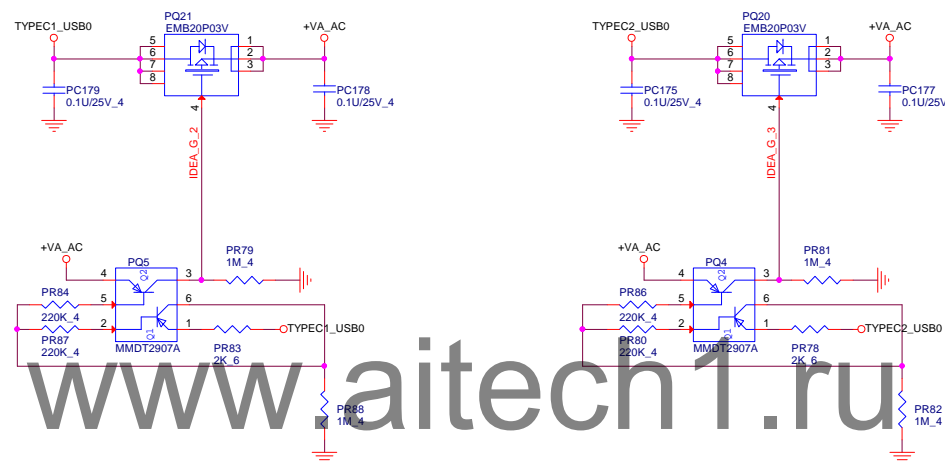
## PortA Dead Battery

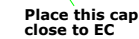
Figure 65. Dead-Battery Condition Flow Diagram  
TI PD TPS65982 Port A

## PortB Dead Battery

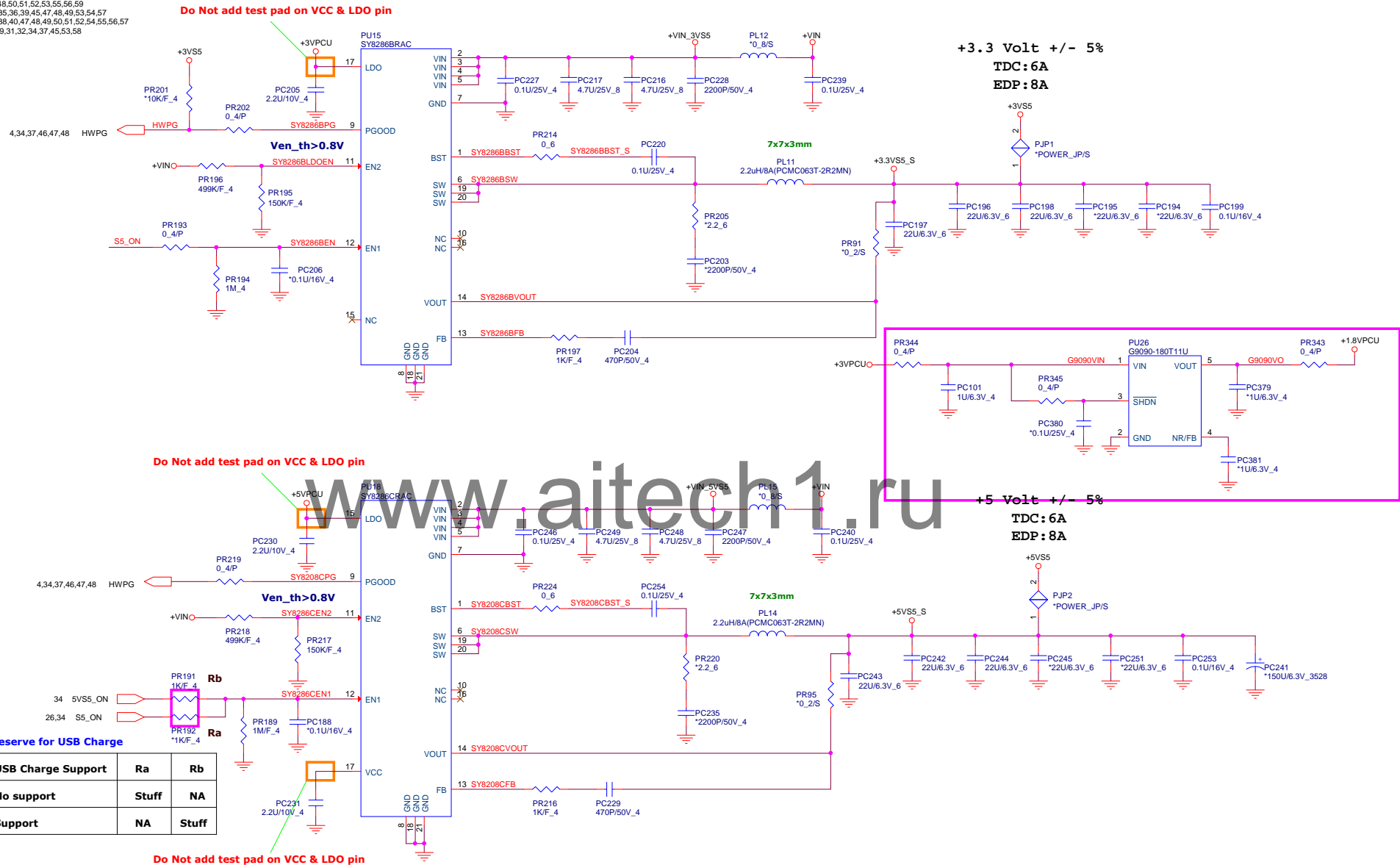


+VA\_AC 45.59  
TYPEC1\_USB0 37  
TYPEC2\_USB0 38

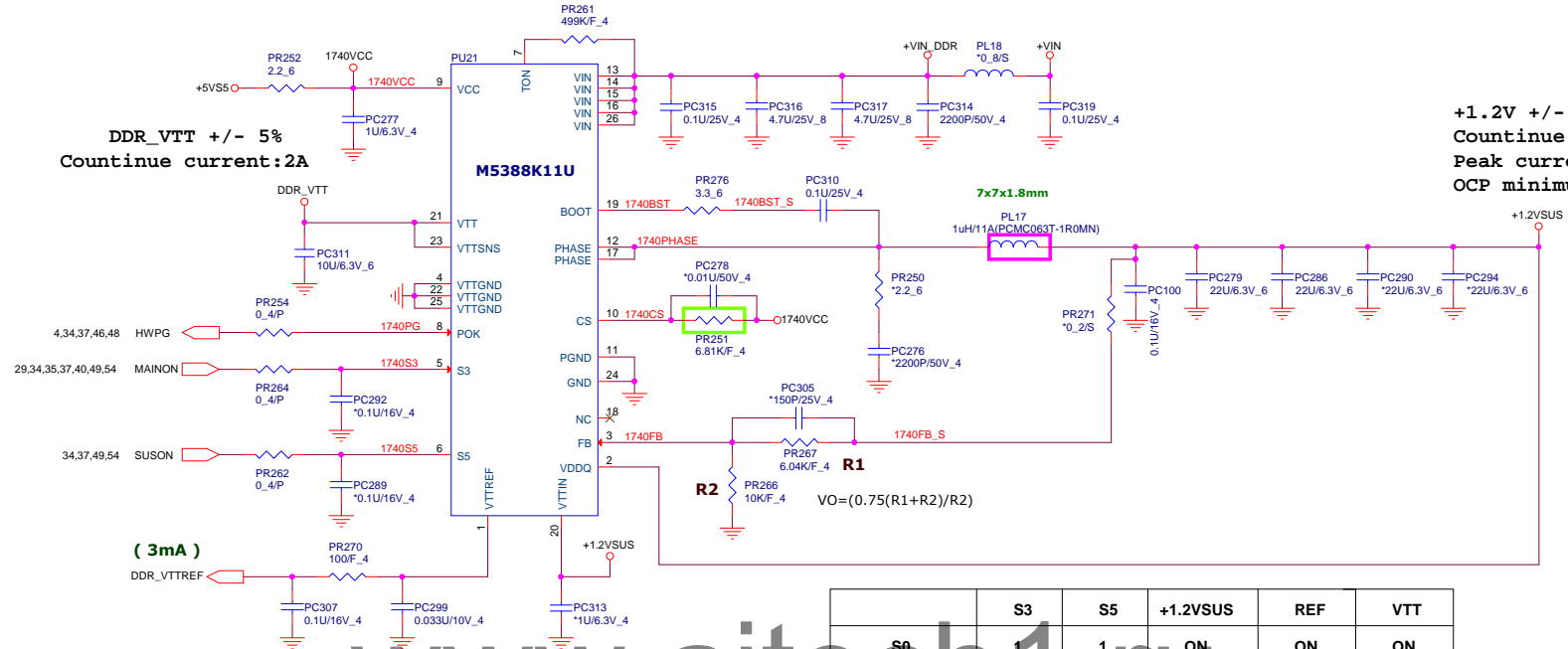




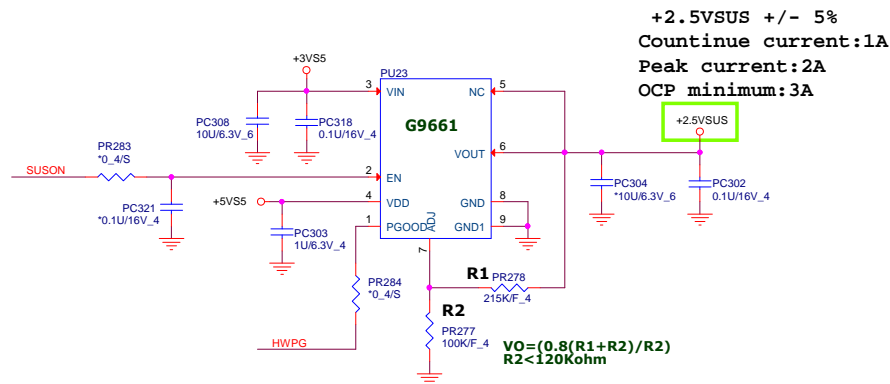
+VIN 23,26,31,45,47,48,50,51,52,53,55,56,59  
 +3VS5 4,15,32,33,34,35,36,39,45,47,48,49,53,54,57  
 +5VS5 4,25,26,29,37,38,40,47,48,49,50,51,52,54,55,56,57  
 +3VPCU 6,13,26,27,29,31,32,34,37,45,53,58  
 +5VPCU 25,26,54,57



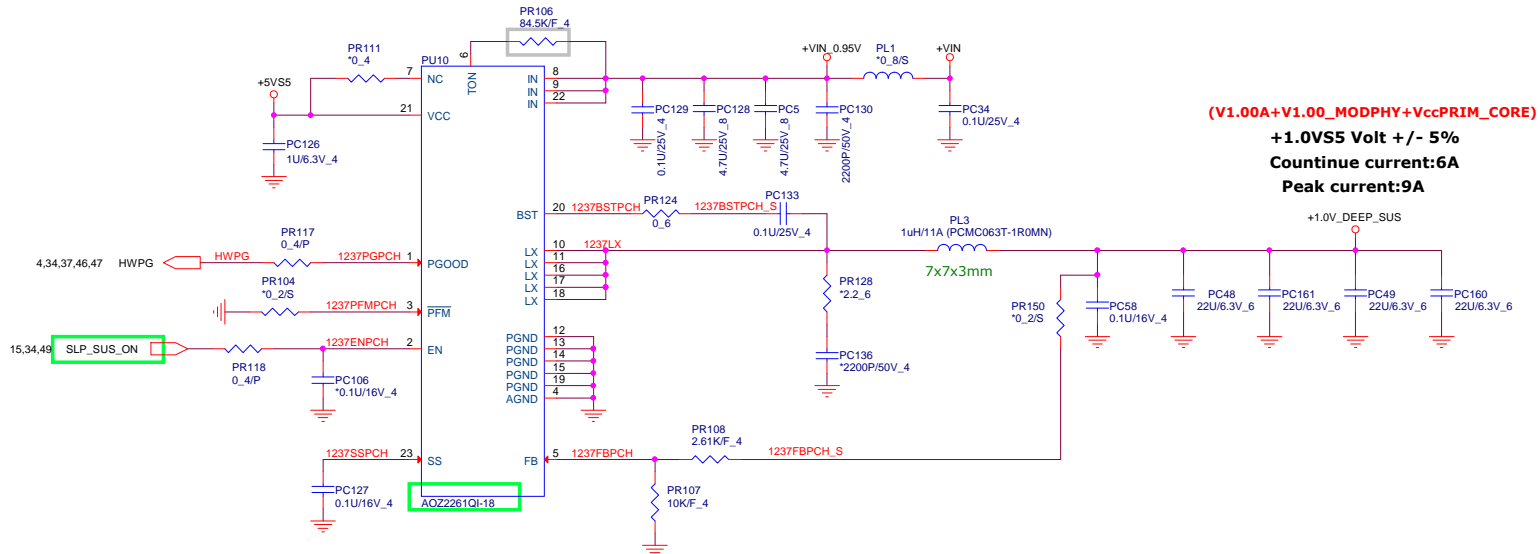
+VIN 23,26,31,45,46,48,50,51,52,53,55,56,59  
 +3VS5 4,15,32,33,34,35,36,39,45,46,48,49,53,54,57  
 +5VS5 4,25,26,29,37,38,40,46,48,49,50,51,52,54,55,56,57  
 +1.2VSUS 3,6,16,17,24,49,57,59  
 DDR\_VTT 16,17  
 +2.5VSUS 16,17



	S3	S5	+1.2VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (main on off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

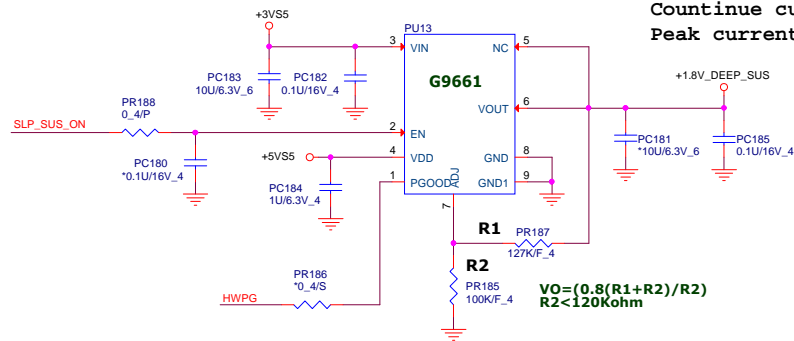


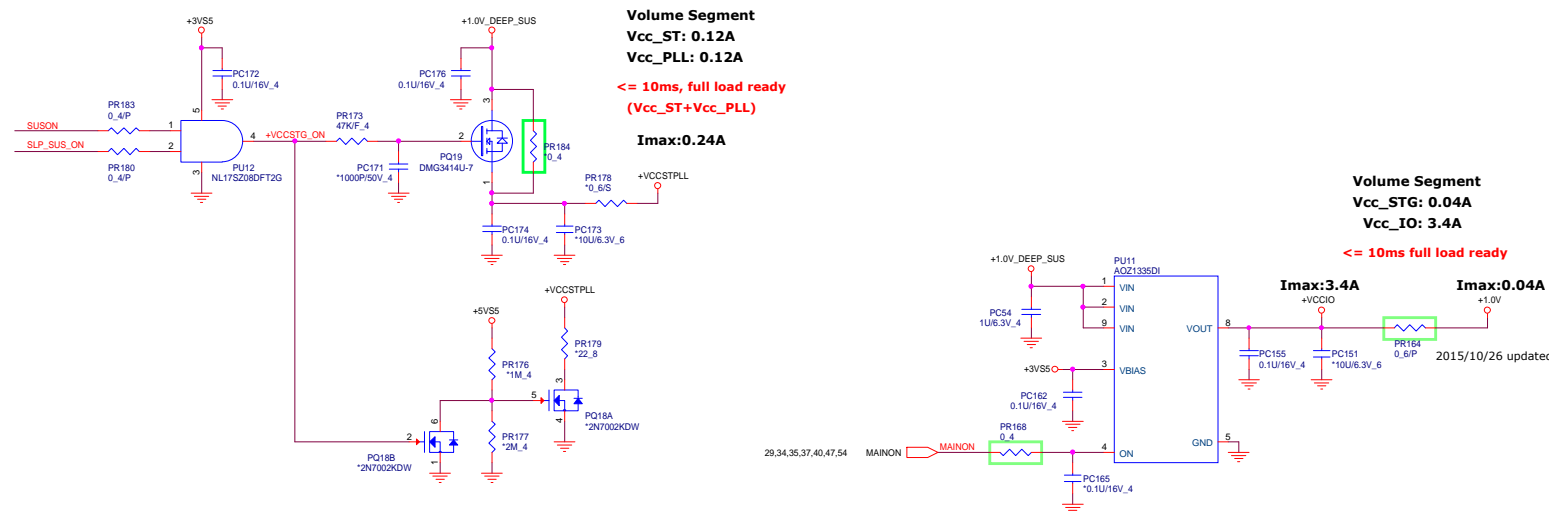
+VIN 23,26,31,45,46,47,50,51,52,53,55,56,59  
 +3VS5 4,15,32,33,34,35,36,39,45,46,47,49,53,54,57  
 +5VS5 4,25,26,29,37,38,40,46,47,49,50,51,52,54,55,56,57  
 +1.0V\_DEEP\_SUS 9,13,15,49  
 +1.8V\_DEEP\_SUS 9,15,45,54



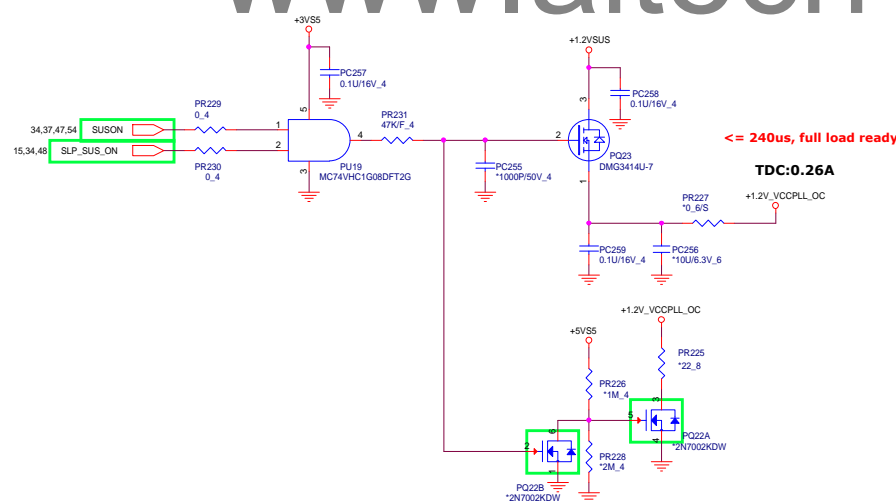
www.aitech1.ru

**+1.8V\_DEEP\_SUS +/- 5%**  
**Countinue current:1.0A**  
**Peak current:3A**

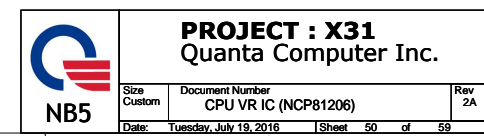




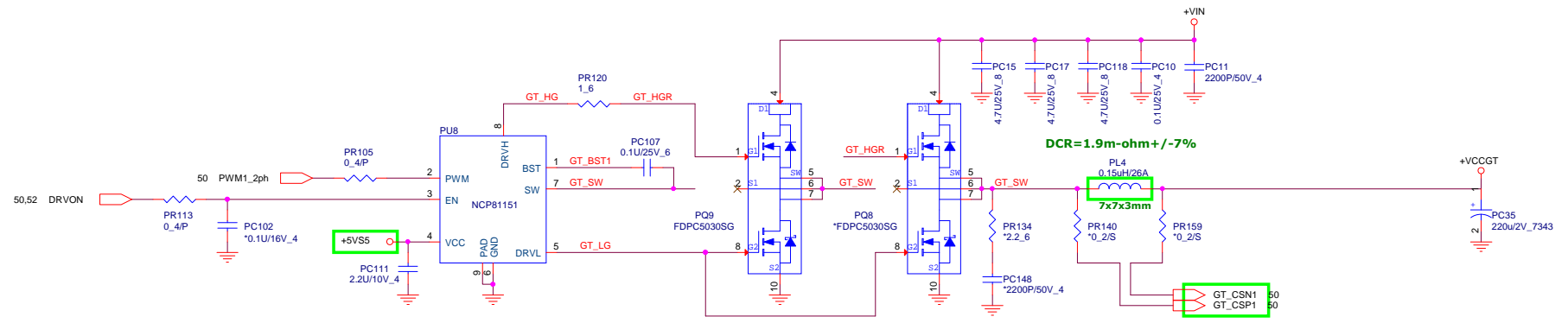
[www.aitech1.ru](http://www.aitech1.ru)





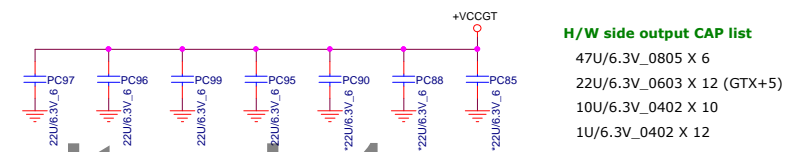


+VIN 23,26,31,45,46,47,48,50,52,53,55,56,59  
+5VSS 4,25,26,29,37,38,40,46,47,48,49,50,52,54,55,56,57  
+VCCGT 7,50



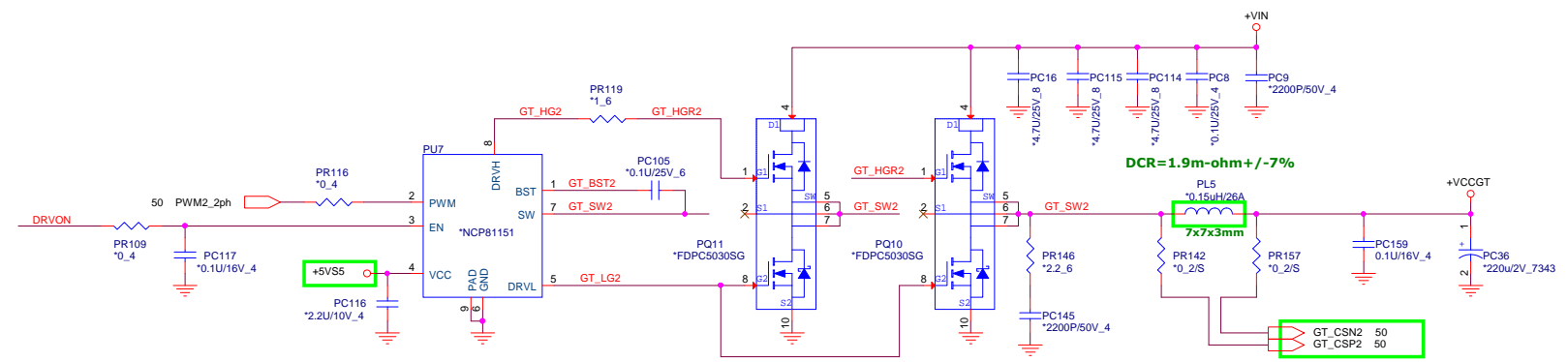
For U23e --> Add These Components

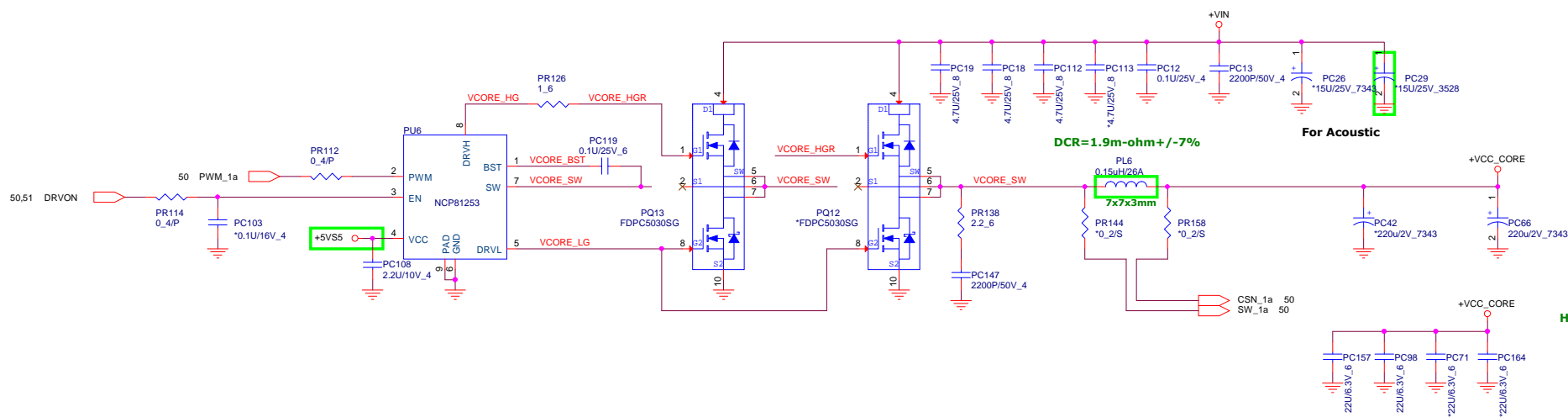
www.aitech1.ru



**H/W side output CAP list**  
47U/6.3V\_0805 X 6  
22U/6.3V\_0603 X 12 (GTX+5)  
10U/6.3V\_0402 X 10  
1U/6.3V\_0402 X 12

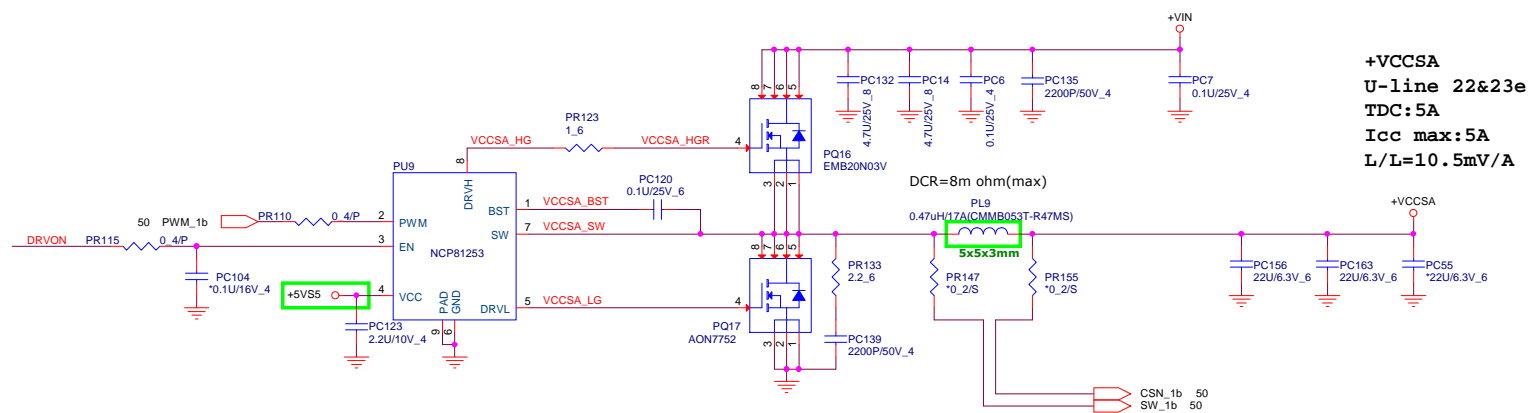
**+VCC\_GT**  
**U-line 22 (15W)**  
TDC:18A(22)  
Icc max:31A(22)  
L/L=3.1mV/A  
**U-line 23e(28W)**  
TDC:35A(23e)  
Icc max =64A(GT+GTx)  
L/L=2mV/A



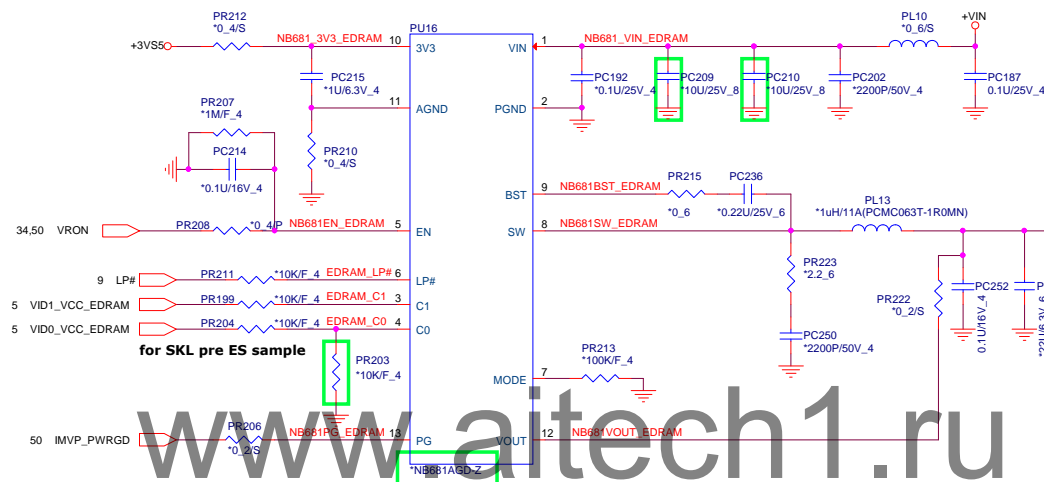
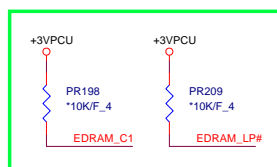


+VIN 23,26,31,45,46,47,48,50,51,53,55,56,59  
 +5VS5 4,25,26,29,37,38,40,46,47,48,49,50,51,54,55,56,57  
 +VCCSA 6,50  
 +VCC\_CORE 5,59

www.aitech1.ru



+VCC\_EDRAM +/- 5%  
 Countinue current:4.5A  
 Peak current:6A



VCC\_EDRAM

LP#	C1	C0	Vout
0	X	X	0
1	0	0	0.8
1	0	1	0.95
1	1	0	1.0
1	1	1	1.05

MODE

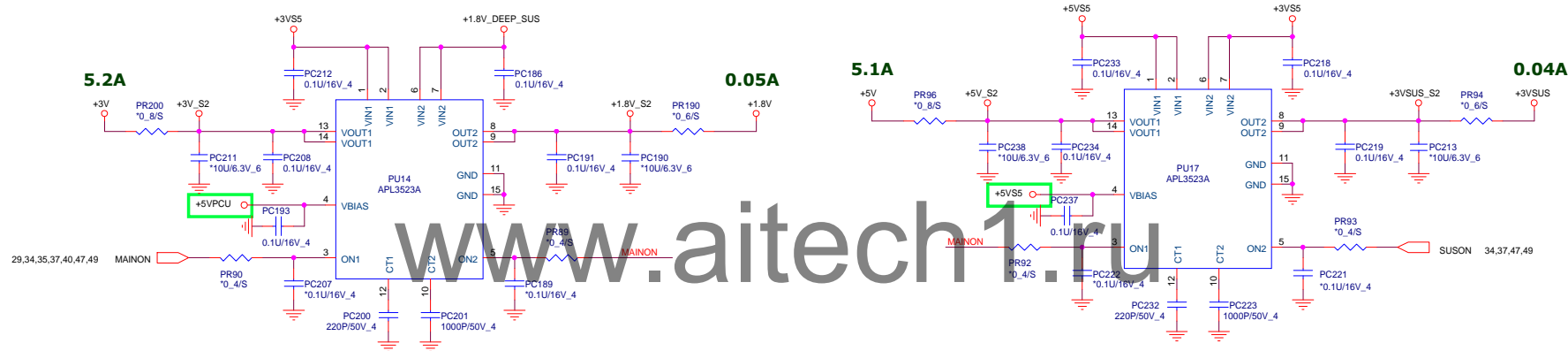
	VR rail	Resistor
M1	VCCIO	0
M2	PRIMCORE	Float
M3	EDRAM/EOPIO	100K
M4	other	150K

+VIN 23,26,31,45,46,47,48,50,51,52,55,56,59  
 +3VS5 4,15,32,33,34,35,36,39,45,46,47,48,49,54,57  
 +3VPCU 6,13,26,27,29,31,32,34,37,45,46,58  
 +VCC\_EOPIO 5  
 +VCC\_EDRAM 5

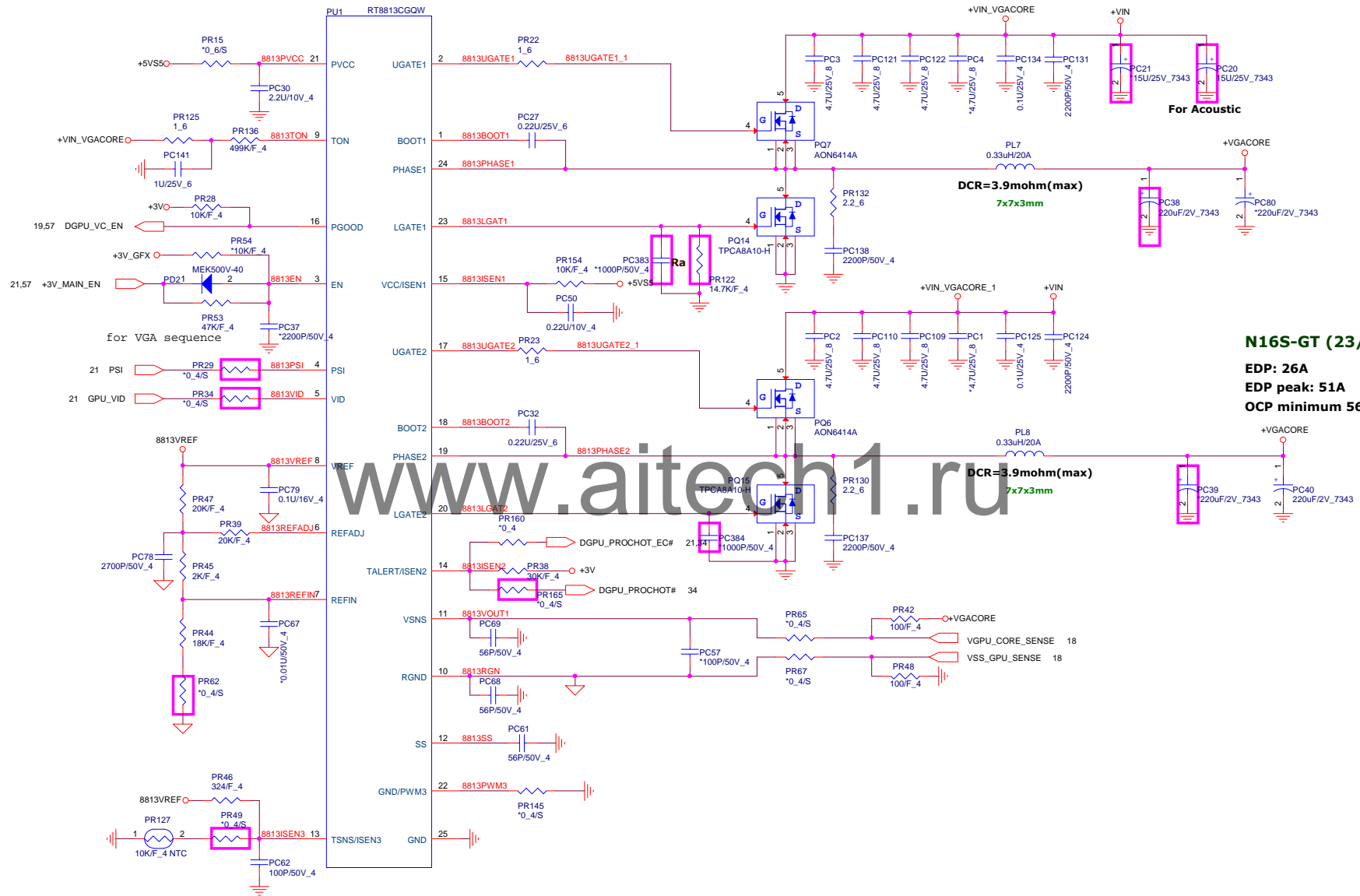


**PROJECT : X31**  
 Quanta Computer Inc.

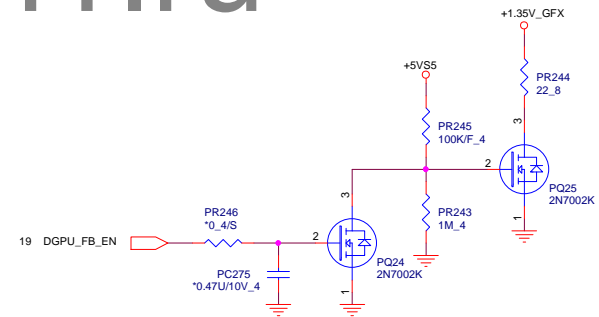
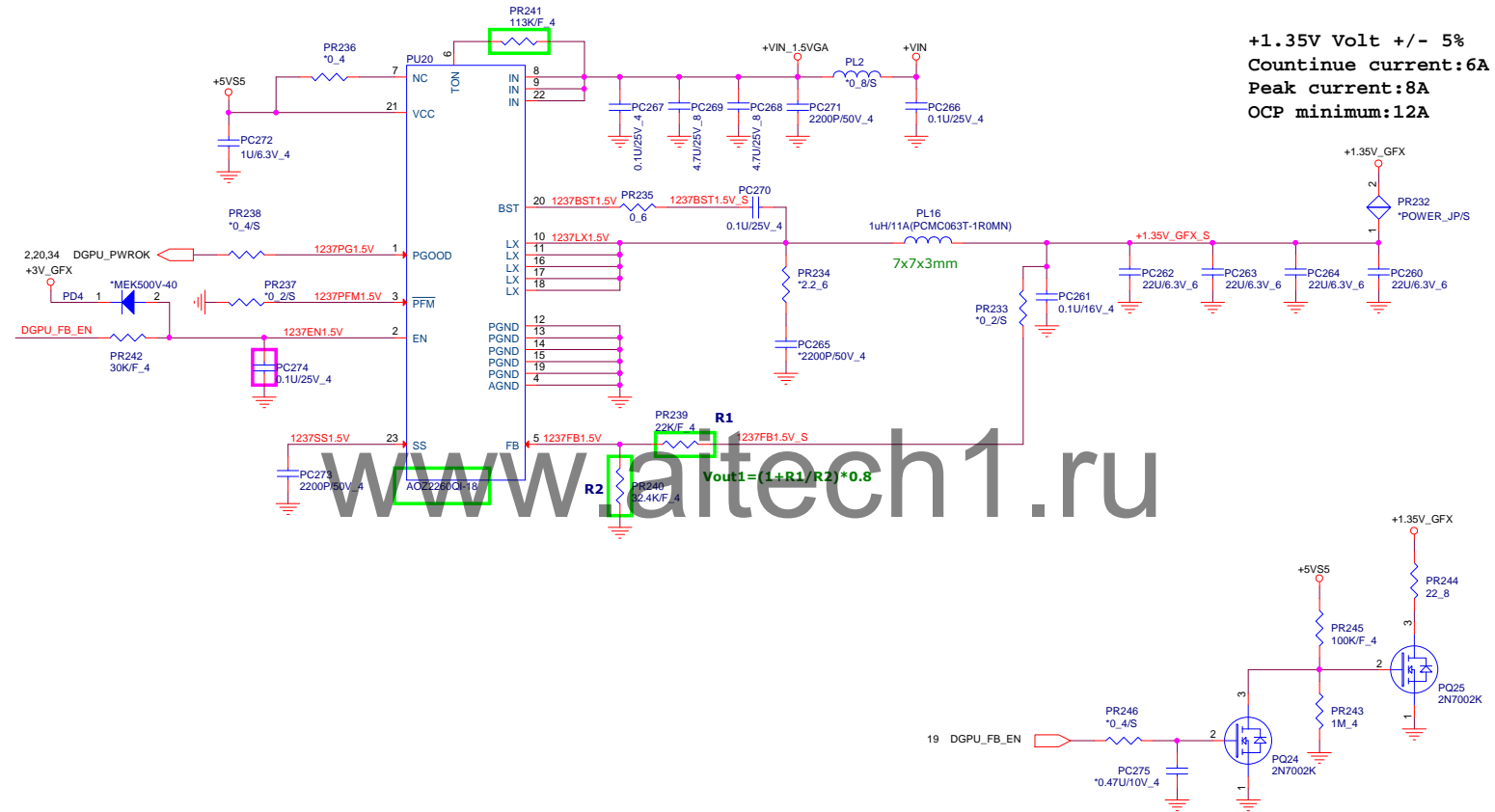
Size	Document Number	Rev
Custom	+VCC_EDRAM (NB681)_23E	
Date: Tuesday, July 19, 2016	Sheet 53 of 59	



+3V 2,4,10,11,12,13,14,15,16,17,19,23,24,25,28,30,31,33,34,35,40,50,54  
 +VIN 23,26,31,45,46,47,48,50,51,52,53,56,59  
 +5VSS 4,25,26,29,37,38,40,46,47,48,49,50,51,52,54,56,57  
 +3V\_GFX 18,20,21,56,57  
 +VGACORE 18

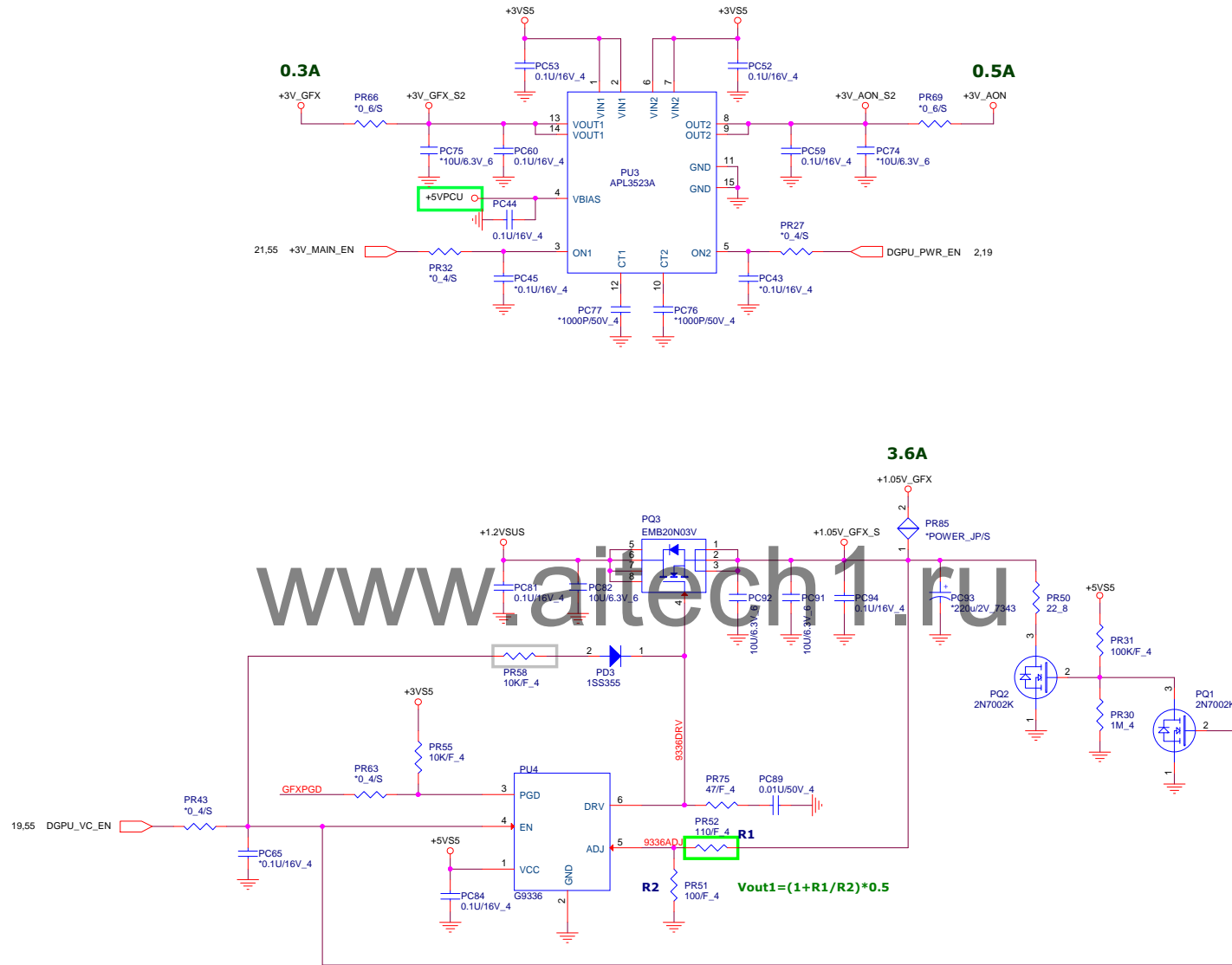


+VIN 23,26,31,45,46,47,48,50,51,52,53,55,59  
 +5VS5 4,25,26,29,37,38,40,46,47,48,49,50,51,52,54,55,57  
 +1.35V\_GFX 19,20,22

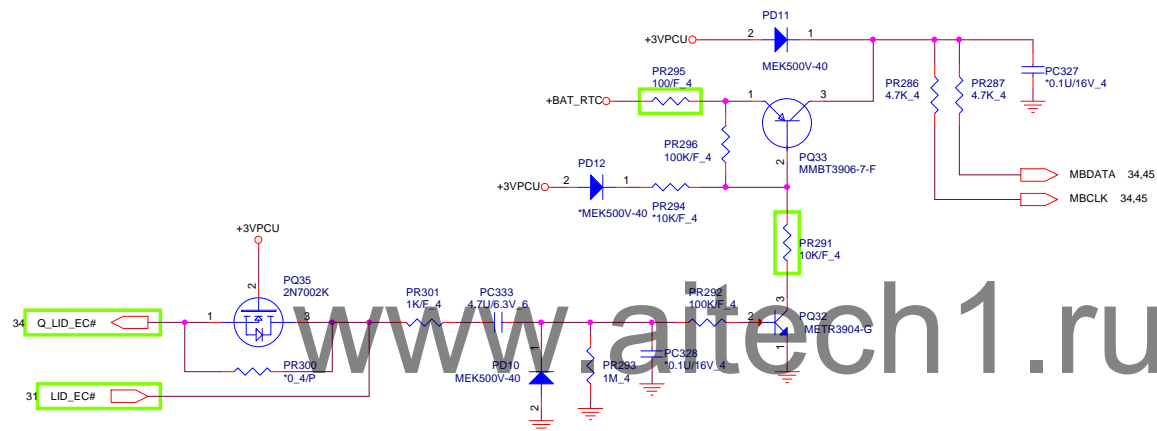




+VIN 23,26,31,45,46,47,48,50,51,52,53,55,56,59  
 +3VS5 4,15,32,33,34,35,36,39,45,46,47,48,49,53,54  
 +5VS5 4,25,26,29,37,38,40,46,47,48,49,50,51,52,54,55,56  
 +3V\_GFX 18,20,21,55,56  
 +3V\_AON 18,20,21  
 +1.2VSUS 3,6,16,17,24,47,49,59  
 +1.05V\_GFX 18,19,20

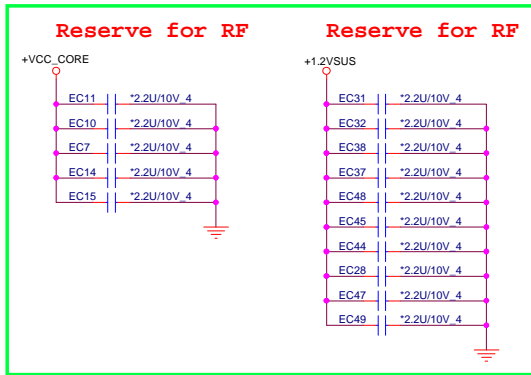


+3VPCU 6,13,26,27,29,31,32,34,37,45,46,53  
+BAT\_RTC 4,13,15,31,45

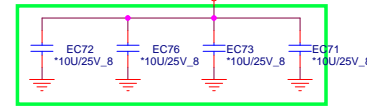


+VIN 23,26,31,45,46,47,48,50,51,52,53,55,56  
+PRWSRC 45  
+VA\_AC 44,45

0329



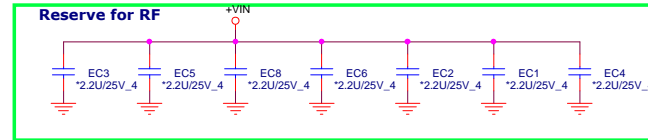
EMI request for ISN +VIN



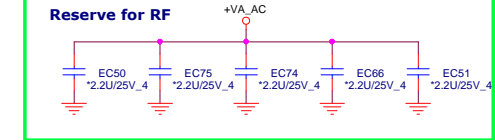
EMI request for ISN +PRWSRC



Reserve for RF +VIN



Reserve for RF +VA\_AC



www.aitech1.ru